"Electronics is defined as the branch of science and technology that deals with flow of current through vaccum and semiconductor devices and their utilization."

Deals with smaller current (power), also deals with bipolar current, it also deals with high freq. (microwave freq)

BASIC DEFINATIONS

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⇒ THERMAL VOLTAGE (V_T) –

"volt equivalent of temperature".

$$\boxed{V_T = \frac{\bar{K}T}{q} \text{ volts.}}$$

T = temperature in kelvin

q = charge = 1.6×10^{-19} C

$\bar{K}$ = Boltzmann constant = 1.38×10^{-23} J/°K

NOTE –

K & $\bar{K}$ (both are boltzmann constant)

$K = 8.62 \times 10^{-5}$ eV/°K

$\bar{K} = 1.381 \times 10^{-23}$ J/°K

By substituting value.

$$\boxed{V_T = \frac{T}{11600} \text{ Volts.}}$$

$$\boxed{V_T \propto T}$$

If T = 0K $V_T = 0$ V

If T = 300K $V_T = 26$ mV

$$\left\{ V_T = \frac{T}{11600} = \frac{300}{11600} = 0.0256 \text{ V} = 26 \text{ mV} \right.$$

- for a large variation in temperature, there will be a small variation in thermal voltage.

- The standard room temperature corresponds to a voltage of 26 mV.

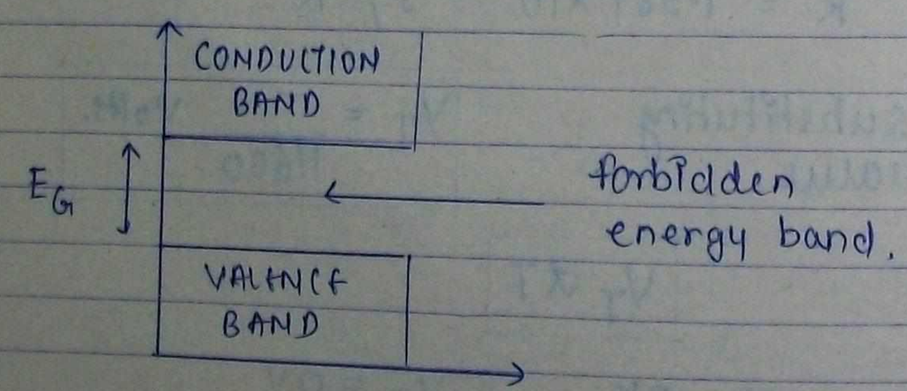
$$\boxed{\text{Temp in } °C = \text{Temp in } K - 273}$$

if $T = 0K = -273°C$ (absolute temp)

if $T = 300K = 27°C$ (standard room temp)

$$\boxed{\text{Temp in } K = \text{Temp in } °C + 273}$$

⇒ **ENERGY GAP (E_G) –**



	Ge	Si
E_{G0} =	0.785 eV	1.21 eV
E_{G300} =	0.72 eV	1.1 eV

$°K \equiv K$

- Energy gap decreases with temperature

$$\boxed{E_G \propto \frac{1}{\text{Temp.}}}$$

- In insulator and semiconductor, energy gap decreases with temperature.

$$\boxed{E_G(T) = E_{G0} - \beta_0 T \quad eV.}$$

β_0 = material constant (eV/K)

for silicon,

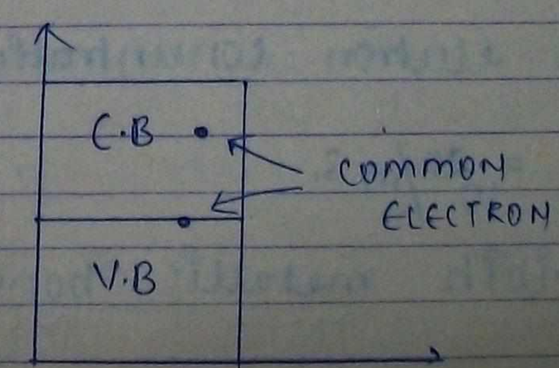
$$E_G(T) = 1.21 - 3.6 \times 10^{-4} T$$

for Germanium,

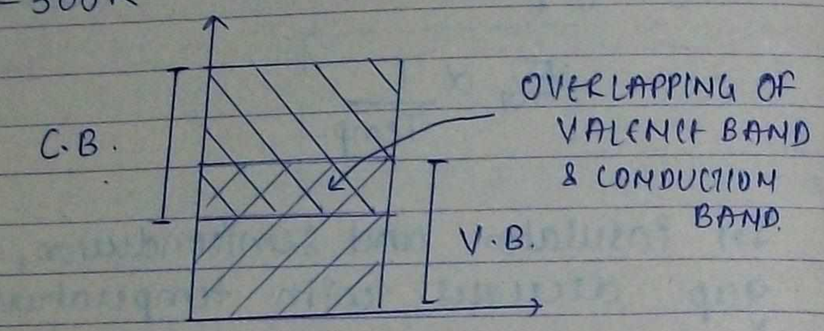
$$E_G(T) = 0.785 - 2.2 \times 10^{-4} T$$

(A) ENERGY GAP OF METALS / CONDUCTORS –

$\boxed{E_G = 0}$ at 0K



At $T = 300K$



This overlapping will increase with temp.

Only metals will have positive temperature coefficient (PTC). of resistance.

$$\boxed{\text{Resistance} \propto \text{Temp.}}$$

Due to overlapping of valence band and cond^n band, metal will exhibit PTC of resistance.

- $\boxed{\text{electron conc. in metals } \eta = 10^{28}/m^3}$

If metal electron concentration is

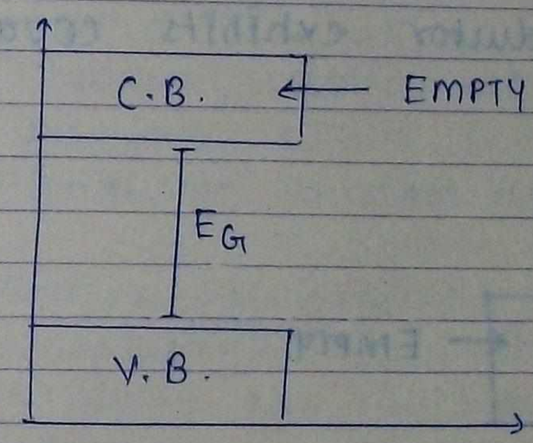
$$\eta = 10^{28}/m^3.$$

- Metal exhibits metallic bonding.

- In metal free electron concentration is independent of temperature.

(B) ENERGY GAPS FOR INSULATORS -

$$\boxed{E_G > 5\,eV} \quad (\text{Large}).$$



- In an insulator no electron can jump from valence band to conduction band and therefore conduction band will be empty i.e. carrier concentration is zero hence conductivity is zero.

- All insulators are bad conductor of current i.e. they do not allow any flow of current through them.

Eg: Plastic, ceramic, SiO_2, Air, mica, PVC, Bakelite

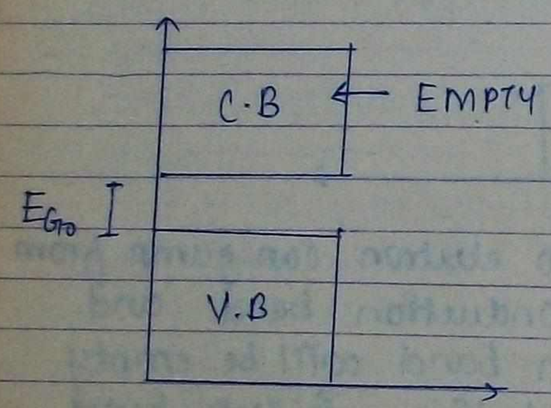
NOTE -
Insulator posseses ionic bonding.

(C) ENERGY GAP OF SEMICONDUCTOR -

$$E_G \simeq 1\ eV\ (0.7 \text{ to } 1.3\ eV)$$

- Semiconductor exhibits covalent bonding.

At T=0K,

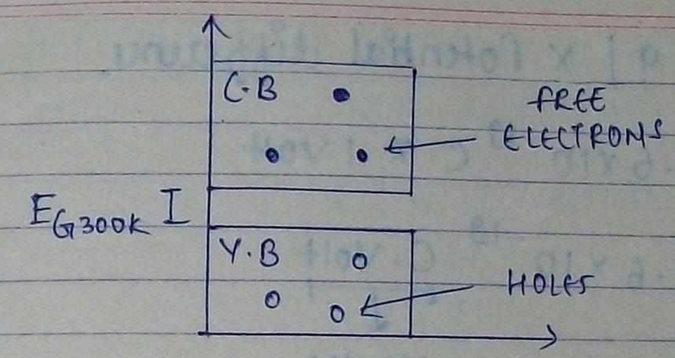


- At T=0K carrier concentrations are zero and therefore conductivity is zero, hence all semiconductors are INSULATORS at 0K.

At room temp T=300K,

(*) Electron can easily pass through vacuum.

(NTC)

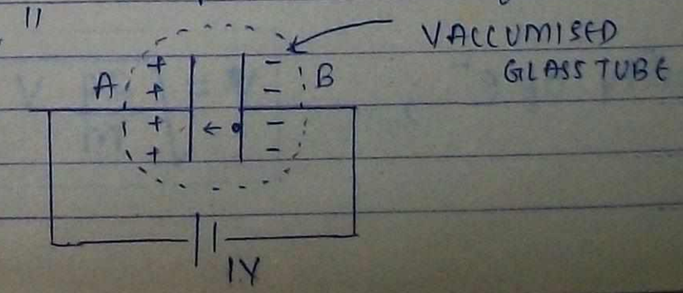


- As temperature increases, covalent bonds will be broken, creating electrons and holes and there will a conductivity in the semiconductor at room temperature.

- Semiconductors are defined as the elements whose conductivity lies in between the conductivity of insulator and cond^ty. of a conductor.

⇒ ELECTRON VOLT (eV) -
It is the practical unit for energy in electronics.

"One electron volt is defined as the energy gain by the electron in moving to a potential difference of one volt."



$1\,eV = |q| \times$ Potential difference.

$= 1.6 \times 10^{-19}\ C \times 1\ volt$

$= 1.6 \times 10^{-19}\ \underbrace{C.Volt}_{\text{Joules}}$

$1\,J = 1\ Nw\text{-}m$

$$\boxed{1\,eV = 1.6 \times 10^{-19}\ Joules.}$$

- Electron volts indicate the amount of kinetic energy gained by the e^- (or) potential energy lost by the e^-.

$KE = \frac{1}{2} m v^2\ J$

$PE = q.V\ J$

KE gained = PE lost by e^-

$\frac{1}{2} m v^2 = qV$

velocity of e^-, $\boxed{v = \sqrt{\frac{2qV}{m}}\ m/sec.}$

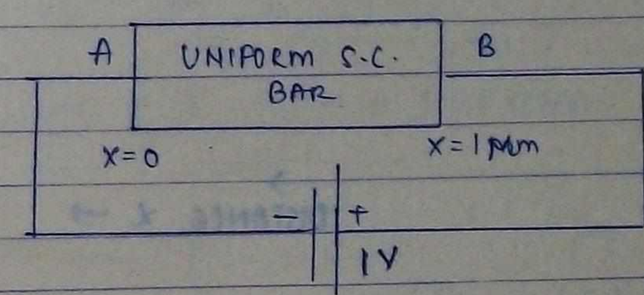
⇒ ELECTRIC FIELD INTENSITY ($\mathcal{E}$ or E) -

FIELD GRADIENT
(OR)
FIELD INTENSITY
(OR)
FIELD.

By defination, $\mathcal{E} = -\frac{dV}{dx}$ Volt/metre

$$\boxed{|\mathcal{E}| = \frac{\text{VOLTAGE EXISTING}}{\text{DISTANCE OR SPACING}}}$$

Considering a uniform semiconductor bar



$|\mathcal{E}|$ at the centre of bar:

$|\mathcal{E}| = \frac{V_c}{x_c}$, $|V_c| = 0.5V$, $x_c = 0.5\,\mu m$

$|\mathcal{E}| = \frac{0.5V}{0.5\,\mu V} = 10^6\ V/m$

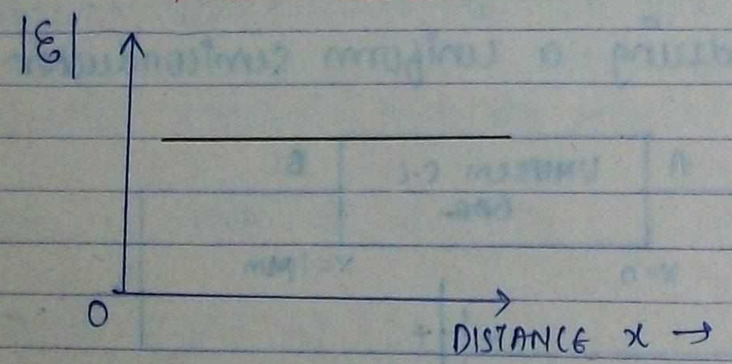
$|\mathcal{E}|$ at the end of bar at B :

$$|\mathcal{E}| = \frac{|V_b|}{X_b} \qquad |V_b| = 1V, \quad X_b = 1\mu m$$

$$|\mathcal{E}| = \frac{1V}{1\times10^{-6}m} = 10^6 V/m.$$

NOTE -

On a uniform semiconductor bar, field intensity will remain constant throughout the bar except at $(x=0)$.



⇒ CURRENT (I) or (i) -

Current is defined as rate of change of charge.

$$\boxed{i = \frac{dq}{dt}} \text{ Amp.}$$

NOTE -

In the semiconductor current is carried by both free electrons and holes.

- when the electrons or holes move the movement is creating the current.

⇒ DRIFT CURRENT -

It is the flow of current to the material or device under the influence of electric field intensity.

⇒ MOBILITY OF CHARGE CARRIERS (μ) -

Mobility denotes how quick is the charge carrier is moving from one place to another place.

By def. $\mu = \frac{\text{DRIFT VELOCITY}}{\text{FIELD INTENSITY}}$

$$\boxed{\mu = \frac{v}{\mathcal{E}}} \quad m^2/Vsec \text{ or } cm^2/Vsec.$$

NOTE -

Drift velocity is always greater than normal velocity.

DRIFT VELOCITY $\boxed{v = \mu\mathcal{E}}$ m/sec.

electron mobility $= \mu_n$

Hole mobility $= \mu_p$

	Ge	Si
μ_n =	3800 $cm^2/Vsec$	1300 $cm^2/Vsec$
μ_p =	1800 $cm^2/Vsec$	500 $cm^2/Vsec$
$\frac{\mu_n}{\mu_p}$ =	2.1 : 1	2.6 : 1

- Electron mobility is always greater than hole mobility because hence electron can travel faster and also contributes more current than a hole.

(Ge)
- Higher conductivity.
- more suitable for High freq. Appl^n (because of larger gain BW. product)

(Si)
- Switching times are small & therefore more suitable for designing of switches.
- High power application, (power electronic)

(*)
- mobility of charge carriers decreases with the temperature.

$$\boxed{\mu \propto T^{-m}}$$

- As temperature increases the atoms in the materials will vibrates and due to their thermal vibrations or thermal agitations, mobility of charge carriers decreases with the temperature.

m = material constant.

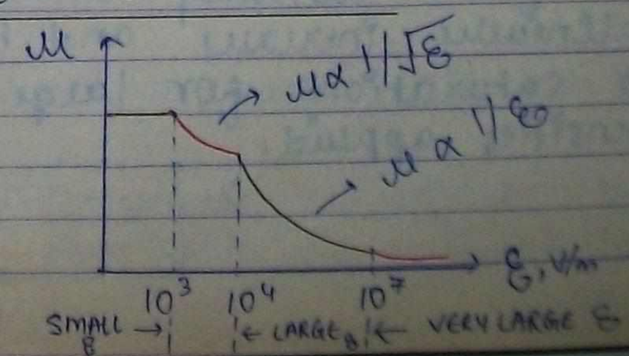
for Ge, m = 1.66 for e^-
m = 2.33 for holes

for Si, m = 2.5 for e^-
m = 2.7 for holes.

- mobility decreases as a non linear variation with the temperature.

μ Vs $\mathcal{E}$ CURVE OF A SEMICONDUCTOR -

Experimentally plotted



$$v = \mu \mathcal{E}$$

$\downarrow\uparrow$ $\quad$ $\downarrow$ CONSTANT

for smaller field intensities applied :

- The mobility of charge carrier will remain constant.

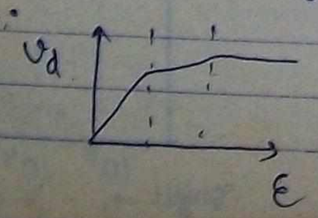
- Drift velocity linearly increases with field intensity.

for larger field intensities applied :

- Mobility of the charge carriers decreases.

- Drift velocity will become constant or its enters into saturations.

- In a semiconductor, as field intensity is increasing the drift velocity will first linearly increases, then sublinearly increases and then enters into saturation for large field intensities applied.



⇒ LEAKAGE CURRENT (I_0) –

MINORITY CARRIER CURRENT.

(OR)

REVERSE SATURATION CURRENT.

(OR)

THERMALLY GENERATED CURRENT.

	Ge	Si
I_0 =	μA	nA

- For better performance of the material or device, leakage currents must be as small as possible.

- The greatest advantage of silicon is smaller leakage current.

- I_0 depends on minority carrier concentration and minority carrier concentration depends on temperature, hence I_0 is very sensitive to temperature.

- for 1°C I_0 increases by approx. 7% both in the Ge and also in Si.

- I_0 doubles for every 10°C rise in temp.

- If leakage currents are small then temp. effect on the material will be less.

therefore the material is having better thermal stability.

- silicon is having better thermal stability than Germanium.

- silicon is more suitable for high temp. applications because of smaller leakage currents.

- I_0 is independent of applied voltage (I_0 is saturated wrt the applied voltage) and therefore it is called saturation current.

$$\boxed{I_0(T_2) = I_0(T_1)\left[2^{\frac{T_2-T_1}{10}}\right] \text{ Amp.}}$$

where, $T_2 > T_1$

⇒ MASS ACTION LAW –

$$\boxed{np = n_i^2}$$

n = conc. of free electrons
p = conc. of holes.
n_i = intrinsic concentration.

(thermal equilibrim = const. temp)

- In a semiconductor (intrinsic & extrinsic) under thermal equilibrim, the product of electrons and holes is always a constant and is equal to the square of intrinsic concentration (n_i).

- The law is mainly used to calculate the concentration of minority carriers.

FOR N-TYPE SEMICONDUCTOR –

majority carrier conc. (electron) $= n_n$

minority carrier conc. (holes) $= p_n$, $\boxed{p_n = \frac{n_i^2}{n_n}}$

FOR P-TYPE SEMICONDUCTOR –

majority carrier conc (holes) $= p_p$.

minority carrier conc (electron) $= n_p$, $\boxed{n_p = \frac{n_i^2}{p_p}}$

MINORITY CARRIER CONC. $= \frac{n_i^2}{\text{MAJORITY CARRIER CONC.}}$

MAJORITY CARRIER CONC. $\propto$ DOPING CONCENTRATION

$$\boxed{\text{MINORITY CARRIER CONC.} \propto \frac{1}{\text{DOPING CONC.}}}$$

⇒ **INTRINSIC CONCENTRATION (n_i) –**

It is the concentration available in the pure semiconductor at a given temperature.

So in intrinsic semiconductor

$$\boxed{n = p = n_i}$$

Equation for intrinsic concentration:

$$n_i^2 = A_0 T^3 e^{-E_{G0}/kT}$$

replacing E_{G0} by E_G:

$$\boxed{n_i^2 = A_0 T^3 e^{-E_G/kT}}$$

$$\boxed{n_i^2 \propto T^3}$$

Que. Intrinsic conc. $n_i \propto$ ----

(1) T^3 (2) $T^{3/2}$

Ans. (2) $T^{3/2}$

$n_i^2 \propto T^3$

$n_i \propto T^{3/2}$

A_0 is a material constant.

- when compare to silicon, Ge. has larger value of n_i and this is due to smaller value of energy gap in the Germanium.

At room temp.,

$n_i = 2.5 \times 10^{13}$ atoms/cm^3 for Ge.

$n_i = 1.5 \times 10^{10}$ atoms/cm^3 for Si.

⇒ **EINSTEIN'S EQUATION –**

In a semiconductor

$$\boxed{\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T = \frac{T}{11600}}$$

$$\boxed{\frac{\mu_n}{D_n} = \frac{\mu_p}{D_p} = \frac{1}{V_T} = \frac{11600}{T}}$$

It gives the relationship between diffusion constant, mobility and thermal voltage.

$$\frac{D}{\mu} \propto T$$

$$\frac{\mu}{D} \propto \frac{1}{T}$$

The unit for mobility to Diffusion constant is V^{-1}

The unit for D/μ is V.

⇒ DIFFUSION CONSTANT OF CHARGE CARRIERS –

electron diffusion constant $\boxed{D_n = \mu_n \cdot V_T}$

hole diffusion constant $\boxed{D_p = \mu_p \cdot V_T}$

unit for diffusion constant is cm^2/sec or m^2/sec.

for Ge, (at 300k)

$D_n = \mu_n \cdot V_T$

$D_n = 3800 \times 26 \times 10^{-3}$

$\boxed{D_n = 99\ cm^2/sec}$ ✓

$D_p = 1800 \times 26 \times 10^{-3}$

$\boxed{D_p = 47\ cm^2/sec}$ ✓

for Si, (at 300k)

$D_n = 34\ cm^2/sec$ ✓

$D_p = 13\ cm^2/sec$ ✓

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for Ge,

$\frac{D_n}{D_p} = 2.1$

for Si,

$\frac{D_n}{D_p} = 2.6$

because, $\frac{D_n}{D_p} = \frac{\mu_n V_T}{\mu_p V_T} = \frac{\mu_n}{\mu_p}$.

– Diffusion constant of charge carrier slightly decreases with the temperature.

$D = \mu V_T$

$\downarrow \quad \downarrow \quad \uparrow$

⇒ POSITIVE TEMPERATURE COEFFICIENT –

Any parameter increasing with the positive temperature.

Ex – V_T, I_0.

⇒ NEGATIVE TEMPERATURE COEFFICIENT –

Any parameter decreasing with temperature

Ex – μ, E_G.

⇒ **RESISTIVITY (ρ) –**
(SPECIFIC RESISTANCE OF MATERIAL)

unit of ρ → Ωcm or Ωm.

for metals –

PTC of resistance
'R' increase with 'T'
($R \propto \rho$) ρ increases with 'T'

for semiconductors –

NTC of resistance
'R' decreases with 'T'
'ρ' decreases with 'T'

⇒ **CONDUCTIVITY (σ) –**
It is the reciprocal of resistivity.

unit of $\sigma = \frac{1}{\Omega m}$ or $\mho/m$ or S/m

- Conductivity denots current carrying capacity of the material or device.

(A)

$$\boxed{\text{CONDUCTIVITY} = \text{CARRIER CONC.} \times \text{CHARGE} \times \text{MOBILITY}}$$

- Conductivity is directly proportional to:
1. carrier concentration.
2. mobility of charge carrier.
3. charge.

IN METALS – (since unipolar)

$$\boxed{\sigma = nq\mu_n} \quad \mho/cm$$

(*) In metals conductivity decreases with temperature.

- In metals as temperature increases, mobility of the charge carriers decreases and therefore conductivity decreases.

- In metals free electron concentration is independent of temperature.

- In metal $\boxed{\sigma \propto \mu_n}$

(B)

IN SEMICONDUCTORS –

$$\boxed{\sigma = nq\mu_n + pq\mu_p} \quad \mho/cm \quad \text{(bipolar)}$$

- In semiconductor conductivity increases with temperature.

- In a semiconductor as temp. increases mobility of charge carrier decreases and this will reduce the conductivity by a smaller value, but at the same time because of thermal energy a large number of covalent bonds will be broken creating large number of electrons and holes and therefore the conductivity increases by a larger value and the net result, the conductivity increases with temp.

- In a semiconductor, conductivity mainly depends upon carrier concentration,

⇒ CURRENT DENSITY (J) -

current passing per unit area

$$J = \frac{I}{Area}$$ Amp/m²

$$J = \sigma E$$ A/cm² ($\mho V m^{-2}$)

IN METALS -

$$J = nq\mu_n E$$ A/cm²

IN SEMICONDUCTOR -

$$J = (nq\mu_n + pq\mu_p) E$$ A/cm²

⇒ CONDUCTIVITY VARIATION IN THE SEMICONDUCTOR -

- In a semiconductor conductivity increases with the temperature.

for 1°C, σ of Ge increases by 6 %

for 1°C, σ of Si increases by 8 %

- when compare to Ge, Si is more sensitive to temp. but Si is used for ~~used~~ high temp. applications and this is due to smaller values of leakage current in the Si.

⇒ OPERATING TEMPERATURES -

for Ge -

−60°C to +75°C

max. operating temp = 75°C (80°C)

for Si -

−60°C to +175°C

max. operating temp = 175°C (180°C

⇒ NORMAL WORKING TEMP –

100k to 400k

⇒ ELECTRICAL PROPERTIES OF Ge & Si. –

PROPERTIES	Ge	Si
1. Atomic no.	32	14
2. Total no. of atoms (density of atoms) /cm³	4.421×10^{22}	5×10^{22}
3. Intrinsic concentration n_i at 300k atom/cm³	2.5×10^{13}	1.5×10^{10}
4. Intrinsic ρ_i Resistivity Ωcm	45	230,000
5. Leakage current (I_0)	μA	nA
6. Max. operating temp	75°C	175°C
7. power handling capacity	LOW	HIGH
8. E_{G0}	0.782	1.21
9. E_{G300}	0.72	1.1
10. μ_n	3800	1300
11. μ_p	1800	500
12. D_n	99	34
13. D_p	47	13

(*) Silicon is cheap and availablity is more than germanium.

– Silicon is more fancy than Ge :

1. Smaller leakage current.
2. High power handling.
3. high temp. applications.
4. Si is plenty available under surface of the earth. (This is the primary reason why silicon is more fancy by S.C. device manufactures).
5. very economical or cheaper.
6. Si can be made into SiO_2 (This is the main reason why silicon is fanced by IC manufactures).

$$Si + O_2 \xrightarrow[\Delta]{1400^\circ C} SiO_2$$

– The main disadvantage of Si is small cond^n.

⇒ GALLIUM ARSENIDE (GaAs) –

Ga As (compound)

3rd group. 5th group

$\mu_n = 5600\ cm^2/Vsec$ to $8500\ cm^2/Vsec$.

$\mu_p = 400\ cm^2/Vsec$

$E_{G300} = 1.47\ eV$.

- It is a compound with Ga. from 3rd group and As. from 5th group.
- It is the best example for direct band gap semiconductor.
- During the recombinations, energy is given out in the form of light.
- The best material for microwave applications.
- GaAs is a low noise material ($\frac{1}{F}$ NOISE)

Ge Si – 500 MHz (max operating freq).

- Alternative material for GaAs is InP.
- GaAs exhibits negative differential mobility, and due to this property it is more fancy for high freq. applications.
- GaAs can be used in the fabrication of:
  1. LED, 2. Tunnel diode, 3. GUNN Diode
  4. PIN, 5. Varactor diode, 6. Microwave ICs.

⇒ NUMERICALS –

Que. If the drift velocity of hole under a field gradient of 100 V/m is 5 m/sec. find its mobility.

Soln:
$$\mu = \frac{v}{\mathcal{E}} = \frac{5}{100} = 0.05\ m^2/Vsec$$

Que. The carrier mobility in a semiconductor is $0.4\ m^2/Vsec$, its diffusion constant at 300 k ?

Soln:
$$D = \mu V_T$$
$$= 0.4 \times (26 \times 10^{-3})$$
$$= 0.0104\ m^2/sec.$$

Que. The minority carrier lifetime and diffusion constant in a S.C. material are 100 μs and $100\ cm^2/sec$, the diffusion length of the charge carrier is ?

$L = \sqrt{D.\tau} = \sqrt{100 \times 100 \times 10^{-6}}$ cm

$= 0.1$ cm.

Qu. A sample of n type S.C have electron density of $6.25 \times 10^{18}/cm^3$ at 300K. If the intrinsitic conc. of charge carrier in the sample is 2.5×10^{13} atoms/cm^3 find the hole conc.

Soln:

$$n_p = \frac{n_i^2}{n_n}$$

$$= \frac{(2.5 \times 10^{13})^2}{6.25 \times 10^{18}} = \underline{\underline{10^8/cm^3}}.$$

Qu. A flat Al strip with the resistivity of $3.44 \times 10^{-8}\ \Omega m$, a cross sectional area of $2 \times 10^{-4}\ mm^2$ and a length of 5 mm, find the voltage drop across the strip, when a current of 50 mA is passing through it.

Soln:

$$V = IR, \quad R = \rho \frac{L}{A}$$

$$V = (50 \times 10^{-3}) \frac{(3.44 \times 10^{-8})(5 \times 10^{-3})}{(2 \times 10^{-4}) \times 10^{-6}}$$

$$V = (50 \times 10^{-3})(0.86\ \Omega)$$

$$V = \underline{43.\ mV}$$

Qu. A S.C wafer is 0.5mm thick, a potential of 100mV is applied across the thickness.

1. What is the electron drift velocity. If the mobility is 0.2 m/Vsec.
2. How much time is required for an e^- to travel across this thickness.

Soln: $\mu = 0.2$ m/Vsec

(1) $$v = \mu \mathcal{E} = 0.2 \times \frac{100 \times 10^{-3}}{0.5 \times 10^{-3}} \frac{V}{m}$$

$$v = 0.2 \times (200) = 40\ m/sec.$$

(2) time taken, $$t = \frac{0.5mm}{40 m/s} = \frac{0.5 \times 10^{-3} m}{40\ m/s}$$

$$= 12.5\ \mu sec$$

Qu. A small conc. of minority carriers are injected into a homogeneous S.C crystal at one point and having an electric field of 10 V/cm is applied across the crystal so that the minority carriers will be moving at distance of 1cm in 20 μsec calculate the mobility in $cm^2/Vsec$.

Soln:

$$\mu = \frac{v}{\mathcal{E}}$$

$$v = \frac{1 \times 10^{-3}}{20 \times 10^{-6}} = \underline{\underline{0.5 \times 10^5}}$$

$$\mu = \frac{0.5 \times 10^5}{10} = \underline{\underline{5000}}\ cm^2/Vsec.$$

Que. In Ge the leakage currents are 5 μA at 10°C find its value if the temp is 25°C.

Soln:

$$I_0(T_2) = I_0(T_1)\left[2^{\frac{T_2-T_1}{10}}\right]$$

$$= 5\times10^{-6}\left[2^{25-10/10}\right]$$

P-7 Q-20

$$= \underline{\underline{14.14\ \mu A}}$$

Que. The e^- conc. in a sample of uniformly doped n-type si at 300 K varies linearly from $10^{17}/cm^3$ at $x=0$ to $6\times10^{16}/cm^3$ at $x=2\ \mu m$. Assume a situation that e^- are supplied to keep this conc. gradient const. with time if electronic charge is 1.6×10^{-19} C & the diffusion const. $D_n = 35\ cm^2/sec$. The current density in the si if no ~~electricity~~ electric field is —

(A) ZERO
(B) $-1120\ A/cm^2$
(C) $-560\ A/cm^2$
(D) $1120\ A/cm$

⇒ DIFFUSION AND DIFFUSION CURRENT —

gradient → $\frac{d}{dx}$

$\frac{dn}{dx}$ = e^- conc. gradient.

$\frac{dp}{dx}$ = hole conc. gradient.

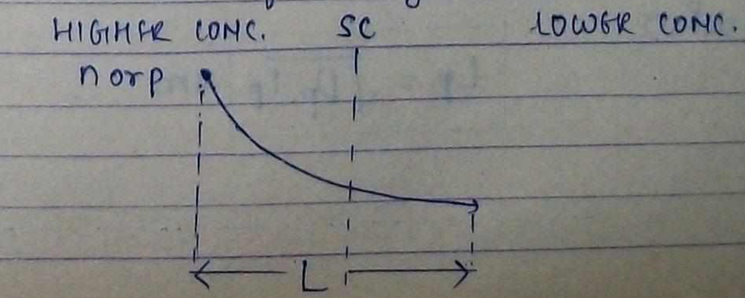
- Diffusion is defined as the migration of charge carriers from higher conc. to lower conc. or from higher density to lower density.

- Diffusion current flow only in s.c.

- Diffusion is mainly due to conc. gradient

- Diffusion is associated with random motion of charge carriers. due to thermal agitations.

- In a semiconductor, diffusion is due to unequal distribution of charge carriers.



length of diffusion, $L = \sqrt{D\tau}$ cm.

D = diffusion constant of charge carrier
τ = carrier life time.

Since $D = \mu V_T$

$$L = \sqrt{\mu V_T \tau} \text{ cm}$$

- The length of diffusion depends on:
  1. Diffusion constant.
  2. Carrier life time.
  3. temperature.
  4. mobility of charge carriers.

- Carrier life time is average life time.

- Diffusion length is average length.

Electron diffusion length $L_n = \sqrt{D_n \tau_n}$ cm

Hole diffusion length $L_p = \sqrt{D_p \tau_p}$ cm

⇒ ELECTRON DIFFUNSION CURRENT DENSITY (J_n) –

$$J_{n(DIFF)} = q D_n \cdot \frac{dn}{dx} \quad A/cm^2$$

⇒ HOLE DIFF. CURRENT DENSITY (J_p) –

$$J_{p(DIFF.)} = -q \cdot D_p \cdot \frac{dp}{dx} \quad A/cm^2$$

- In the above equations the ~~ma~~ charge is the magnitude of charge.

- Diffusion constant is the material constant exhibiting or associated with the property called diffusion.

electron diffusion current. $I_{n(DIFF)} = J_{n(DIFF)} \times Area$

hole diffusion current $I_{p(DIFF)} = J_{p(DIFF)} \times Area.$

- By default always considered area to be $1 cm^2$ or $1 m^2$.

⇒ TOTAL CURRENT DENSITY IN THE SEMICONDUCTOR -

$$J = J_n + J_p \quad A/cm^2$$

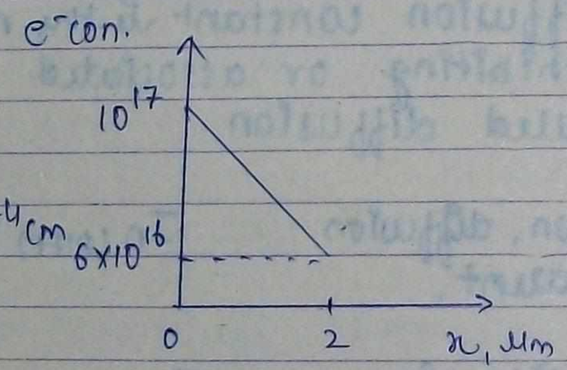
Here, $J_n = J_{n(DRIFT)} + J_{n(DIFF.)}$

$$\boxed{J_n = nq\mu\mathcal{E} + qD_n \cdot \frac{dn}{dx}}$$

also, $J_p = J_{p(DRIFT)} + J_{p(DIFF.)}$

$$\boxed{J_p = pq\mu\mathcal{E} - qD_p \frac{dp}{dx}}$$

Sol^n:



$x = 2\mu m = 2\times10^{-4} cm$

e^- current density

$$J_n = J_{n(DRIFT)} + J_{n(DIFF)}$$

Since $\mathcal{E} = 0$, $J_{n(DRIFT)} = 0$

$$J_n = J_{n(DIFF)}$$
$$= q \cdot D_n \frac{dn}{dx}$$
$$= 1.6\times10^{-19} \times 35 \times \left(\frac{6\times10^{16} - 10^{17}}{2\times10^{-4} - 0}\right) = -1120 A/cm^2$$

P-4
Q-4

Que. e^- mobility & life time in a S.C. at room temp are $0.36 m^2/Vsec$ and $340 \mu s$ resp. The diffusion length is _?

Sol:
$$\mu = 0.36 m^2/Vsec$$
$$\tau = 340 \mu s$$

$$L = \sqrt{\mu \cdot V_T \cdot \tau} = \sqrt{0.36 \times 26\times10^{-3} \times 340\times10^{-6}}$$
$$= 1.77 mm.$$

Que. On applying an electric field of intensity $10 V/cm$ across a S.C. at a certain temp, the average drift velocity of the free e^- is $7000 cm/sec$, the mobility is _?

(1) $7\times10^4 cm^2/Vsec$
(2) $700 cm^2/Vsec$
(3) $7 m^2/Vsec$
(4) $700 cm/Vsec$

Sol^n: $V = \mu\mathcal{E}$

Que. The diffusion constant for holes in Si is $13 cm^2/sec$, what is the diffusion current if the gradient of the whole conc. $\frac{dp}{dx} = -2\times10^{14}$ holes/cm^3/cm

(1) $0.416 \mu A$
(2) $-3.2\times10^{-5} A$
(3) $32 \mu A$
(4) $+0.416 mA$

Sol^n:

$$J_p = -q D_p \frac{dP}{dx}$$

$$= -(1.6 \times 10^{-19})(13)(-2 \times 10^{14})$$

$$= 0.416 \text{ mA/cm}^2$$

$$I_{P(DIFF)} = J_{P(DIFF)} \times \text{area}$$

$$= 0.416 \text{ mA/cm}^2 \times 1 \text{ cm}^2$$

$$= 0.416 \text{ mA.}$$

Que. Given that at room temp the volt equivalent of temp is 26 mV, hole mobility is 500 $m^2/V\,sec$ and life time of the holes is 130 nsec. what is the diffusion length of holes?

Sol^n:

$$L = \sqrt{\mu V_T \tau}$$

$$L = \sqrt{500 \times 26 \times (130 \times 10^{-9})}$$

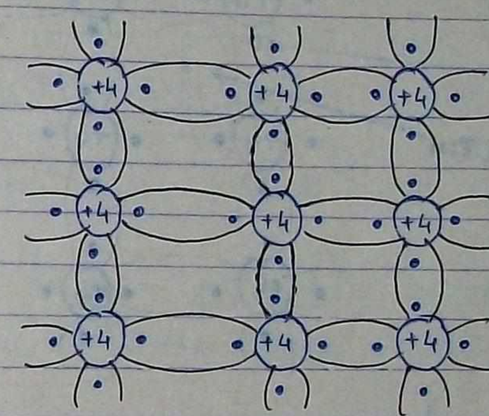
$$L = 1300 \text{ micron } (\mu m)$$

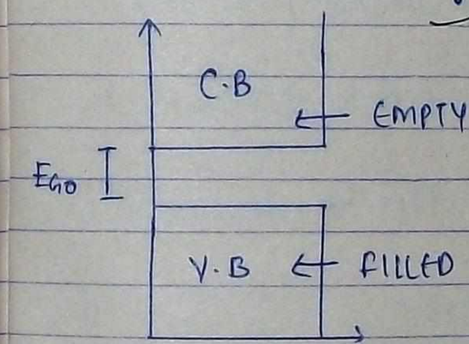
⇒ INTRINSIC SEMICONDUCTOR –

(Pure semiconductor)
or
(Non-degenerative s.c.)

$$n = p = n_i$$

Crystalline structure at 0K



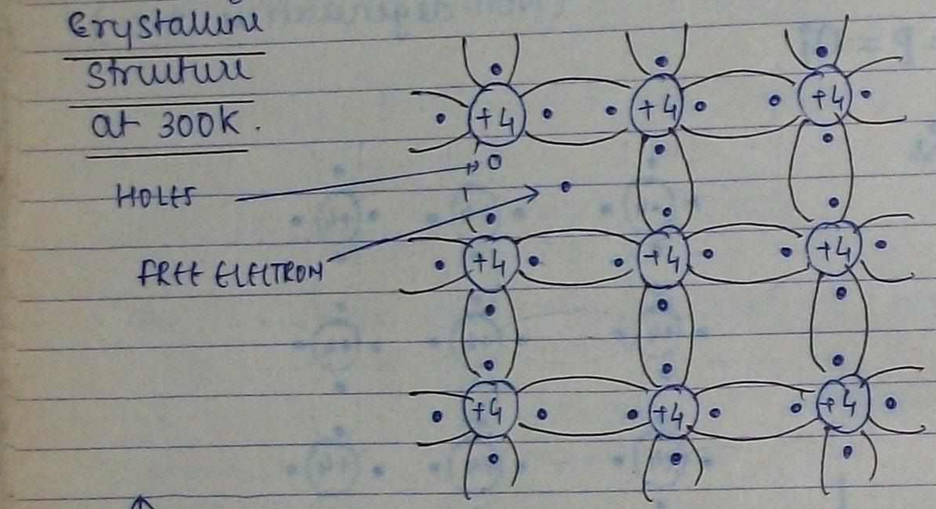


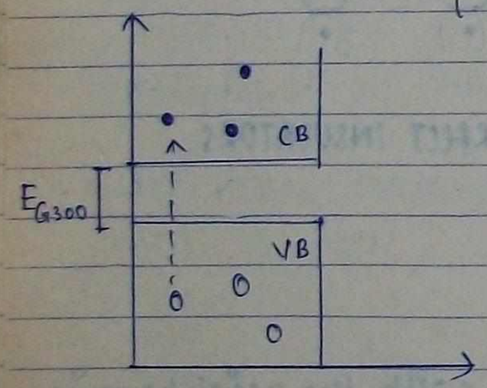
PERFECT INSULATORS

- The sharing of electrons with the neighbouring atoms is called covalent bonding.
- In one covalent bonding there will be two electrons
- At 0K all valency electrons are in perfect covalent bonding

- Intrinsic semiconductor at 0k will behaves as a perfect insulator.

Crystalline structure at 300k.





- when a covalent bond is broken, it create one e^- and one hole (the e^- will be jumping from V.B to C.B and becomes a free electron and the hole will remain in the valence band)

- Hole is deficiency of electron in the broken covalent bond.

- Hole is a carrier of current with a positive charge of 1.6×10^{-19} C.

- The condition for intrinsic S.C is:

$$\boxed{n = p = n_i}$$

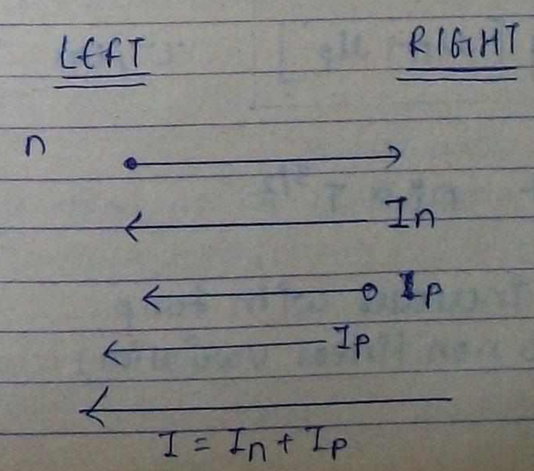
- free electron is also called conduction band e^-.

- Because of opposite polarities electrons & holes always move in the opposite direction.

- Current direction is opposite to the flow of e^-

- current direction is in the direction of hole flow.

In a S.C.



$I = I_n + I_p$
but $I_n > I_p$

- In a semiconductor e^- and hole will be moving in the opposite direction but they contribute the current in the same direction.

- In a S.C the free e^- will be moving in the conduction band and will contribute the current and at the same time the holes will be moving in the valence band and will contribute the current and the total current,

$$I = I_n + I_p.$$

- The conductivity of intrinsic semiconductor.

$$\sigma_i = nq\mu_n + pq\mu_p \quad \mho/cm$$

but $n = p = n_i$

$$\boxed{\sigma_i = n_i q [\mu_n + \mu_p]} \quad \mho/cm$$

$\sigma_i \propto n_i$ but $n_i \propto T^{3/2}$

$\sigma_i \propto T^{3/2}$ (σ_i increases with temp as a non linear variation)

- In intrinsic S.C. conductivity increases with the temp.

- Intrinsic resistivity decreases with the temperature.

$$\rho_i = \frac{1}{\sigma_i}$$

$$\boxed{\rho_i = \frac{1}{n_i q [\mu_n + \mu_p]}}$$

- Conductivity is very less in intrinsic semiconductor (major disadvantage).

⇒ GENERATION OF ELECTRON - HOLE PAIR -
(also called IONIZATION)

- It refers to creating of electrons & holes by breaking the covalent bonds.

⇒ RECOMBINATION -
whenever the free e^- can combine with the hole, it is called recombination.
It refers to a free e^- pairing with the holes.

- During the recombination the free e^- and holes will simultaneously dissapear and a covalent bond is formed.

- During the recombination the free e^- will be falling from conduction band to the valence band to recombine with the hole and energy will be dissipated in the form of heat and light.

⇒ CARRIER LIFE TIME (τ) -
(μsec to nsec)

- It is the average life time of the charge carriers.

- τ is in the range of nsec to μsec.

- Carrier life time is the time taken from breaking of covalent bond until its recombination.

(*) NOTE -
In reality hole is a valency electron, taken with a positive charge.

17/7/11

⇒ DOPING -
It is the process of adding impurities to the pure semiconductor.

- Doping increases carrier concentration and therefore increases the conductivity.

(*) TRIVALENT / ACCEPTOR IMPURITES - B, Al, Ga & In

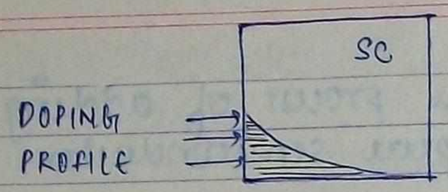
(*) PENTAVALENT / DONAR IMPURITIES - P, As, Sb & Bi

- B & P have more electron affinity toward Si.

- The doping profile can be homogenous or non-homogenous in the nature.

- The doping profile must bring built in electric field in the S.C or must introduced internal electric field (built in electric field) in the SC. So that there will be a drift current in the semiconductor.

- The doping profile will be maximum at the surface where, it is introduce in the S.C. and the profile gradually decrease into the depth of the semiconductor.



1 in 10^6
$1 : 10^6$ or $1/10^6$

⇒ STANDARD DOPING LEVEL –

① MODERATE DOPING – $1 : (10^6 \text{ to } 10^8)$ [P or N]

② LIGHTLY DOPED – $1 : 10^{11}$. [P^- or N^-]

③ HIGHLY DOPED – $1 : 10^3$. [P^+ or N^+]

- The minimum doping required to convert intrinsic semiconductor into extrinsic semiconductor is $1 : 10^8$

- In Ge, with $1 : 10^8$ doping, conductivity increase by 12 time.

- In Ge, with $1 : 10^7$ doping, conductivity increase by 120 time.

⇒ EXTRINSIC SEMICONDUCTOR –

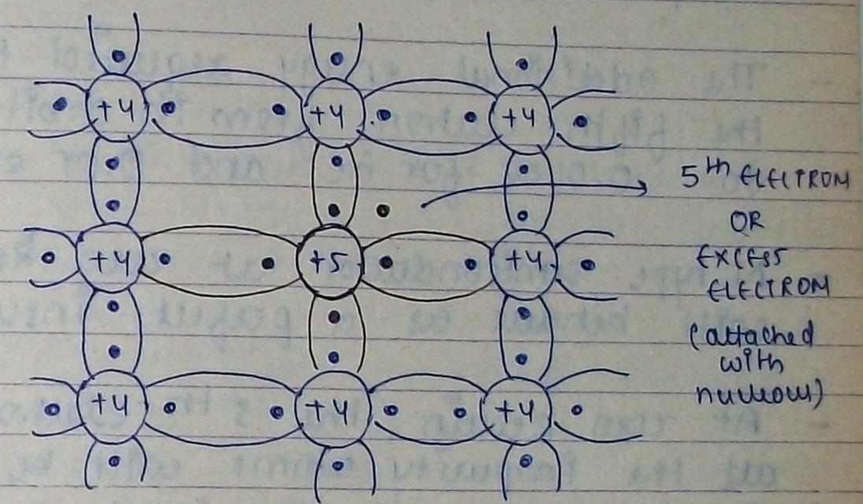
(DOPED SEMICONDUCTOR)
OR
(ARTIFICAL SEMICONDUCTOR)
OR
(IMPURITY SEMICONDUCTOR)

OR
(DEGENERATED S.C.)
OR
(COMPENSATED S.C)

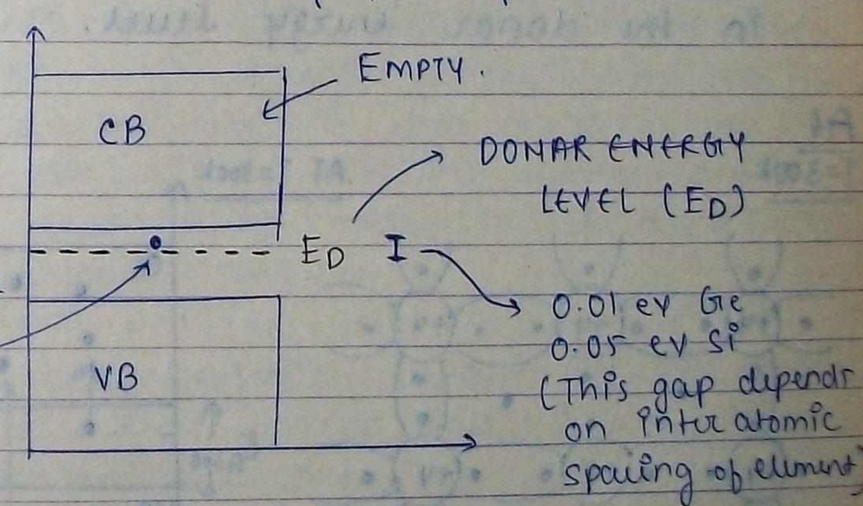
⇒ N-TYPE SEMICONDUCTOR / DONAR –

- The impurity is pentavalent

AT T=0K



AT T=0K



- Donar energy level is a discrete energy level created just below the conduction band.

- Donor energy level represents the energy level of pentavalent atom added to the pure semiconductor.

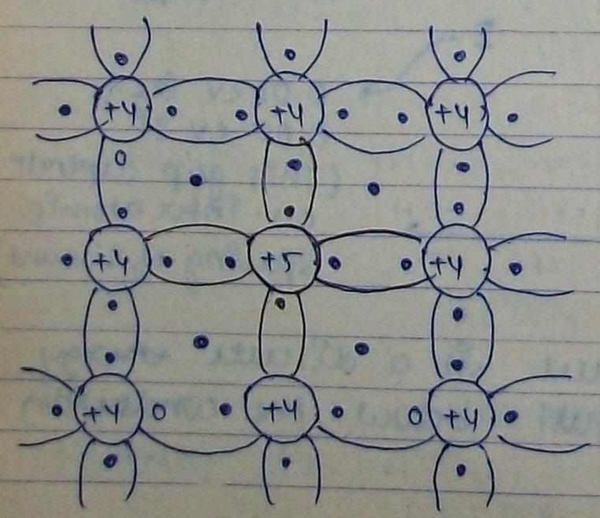
- The additional energy required to detach the fifth electron from its orbit is equal to 0.01 eV for Ge and 0.05 eV for Si.

- N type semiconductor at zero kelvin will behave as a perfect insulator.

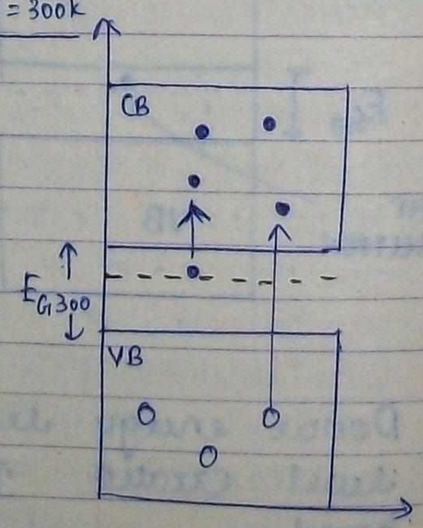
- At zero kelvin, the 5th electron of all the impurity atoms will be existing in the donor energy level.

At
T=300k

$n >> p$



AT T=300k



- In n-type semiconductor every impurity atom will be donating one electron into the conduction band. (Hence n type is also called DONAR).

- In n-type semiconductor as temperature increases 5th electrons will be moving from donor energy level into the conduction band and becomes free electrons and also due to the thermal energy a no. of covalent bonds will be broken creating electrons and holes (equal. no.) and these electrons will be moving from the valence band to conduction band and therefore the electron concentration in the conduction band is far greater than the hole concentration in the valence band and electrons are majority carriers & holes are minority carriers.

- Donor level ionization means the 5th electrons moving from donor energy level into the conduction band.

- Donor level ionization increases with temp. (as temperature increases from 0°K to 300K the 5th electrons of the impurity atoms will be moving from donor energy level into the conduction band.

- At 300 K, donar level ionization is completed.

- Above 300K, there is no donar level ionization.

- Majority carriers will contribute more current with less noise.

- minority carriers will contribute less current and more noise.

- minority carrier noise is thermal noise (and it increases with the temp.)

- The condition for n type semiconductor is:

$$\boxed{n > n_i} \qquad \boxed{p < n_i}$$

- In n type semiconductor as temperature increases, electron concentration increases above n_i and hole concentration fall below n_i and this is due to a large no. of recombinations.

- According to the law of electrical neutrality

$$\boxed{N_D + P = N_A + n}$$

In a n type semiconductor ($N_A = 0$)

$$\boxed{n = N_D + P} \quad \text{(exact eqn)}$$

Since $n \gg P$ $\quad \boxed{n \simeq N_D}$

- N_D is called donar concentration and its denotes the no. of pentavalent atoms added to the pure semiconductor.

$$\boxed{N_D = \text{TOTAL NO. OF ATOMS}/cm^3 \times \text{IMPURITY RATIO}}$$

- In n-type semiconductor, the free electron concentration is approximatly equal to donar concentration. ($n \simeq N_D$).

- In the n-type semiconductor, the current is predominantly, dominated by the flow of electron.

- The conductivity due to minority carriers is almost negligble.

- The conductivity of the n type semiconductor is

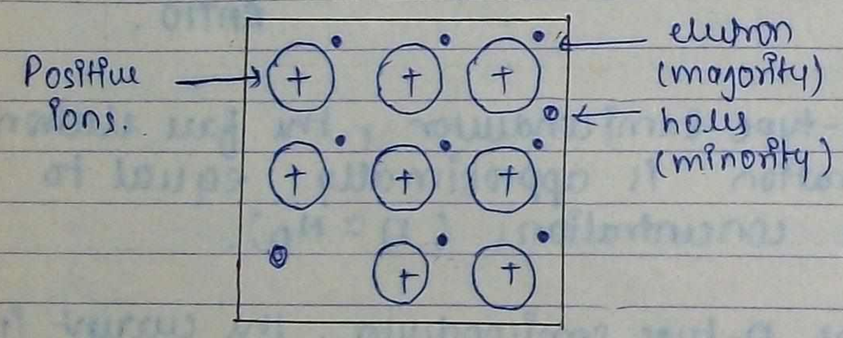
$$\sigma_N = nq\mu_n + pq\mu_p \quad \mho/cm$$

$$\sigma_N \simeq nq\mu_n \simeq N_D q\mu_n \quad \mho/cm$$

⇒ REPRESENTATION FOR N-TYPE SEMICONDUCTOR –

- In n-type semiconductor the impurity atom after donating an electron will be losing the negative charge or gaining the positive charge and it becomes a positive ion.

- Positive ion means a neutral atom with one or more detached electron.



Consider a Si material subjected to donar impurities of $1:10^6$

$$N_D = 5\times10^{22}\ \text{atom/cm}^2 \times \frac{1}{10^6}$$
$$= 5\times10^{16}\ \text{atom/cm}^3$$

ie no. of pentavalent atoms added to the pure semiconductor is $5\times10^{16}\ \frac{\text{atom}}{\text{cm}^3}$

No. of 5th e^- moving from E_D to conduction band $= 5\times10^{16}$ atom/cm³

Due to thermal energy let 10^6 covalent bonds are broken. Hence,

10^6 e/cm³ and 10^6 holes/cm³ are created.

No. of electron moving from valence band to conduction band is 10^6/cm³

Total no of e^- in C.B $= 5\times10^{16}/\text{cm}^3 + 10^6/\text{cm}^3$
$\cong 5\times10^{16}/\text{cm}^3$

Total no of holes in V.B $= 10^6/\text{cm}^3$

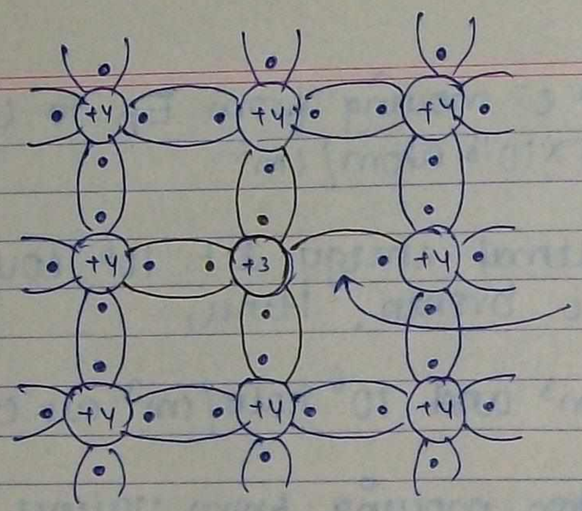
thus, $\boxed{n >> p}$

⇒ P-TYPE SEMICONDUCTOR / ACCEPTORS –

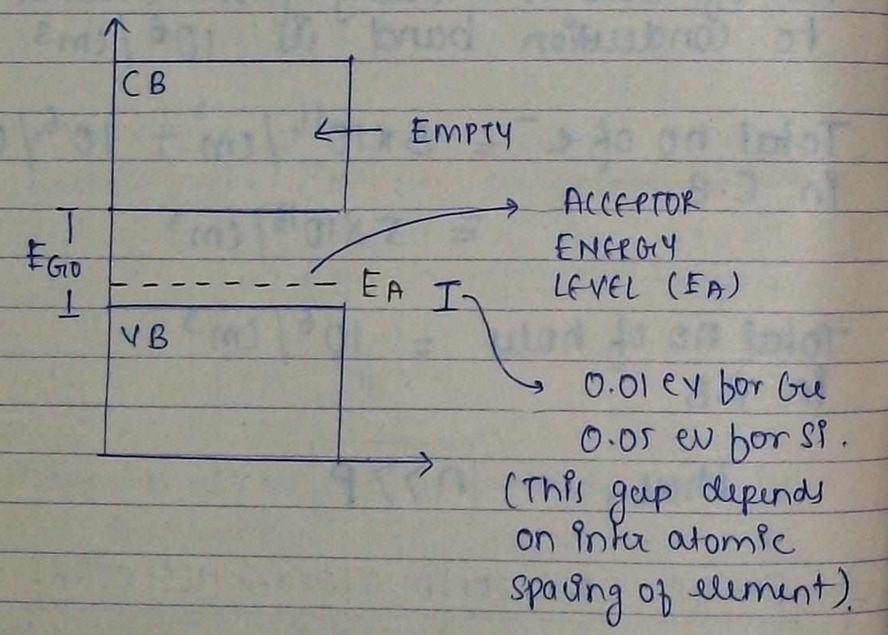
- The impurity is trivalent.

- Acceptor energy level is a discrete energy level created just above the valence band.

AT T=0k



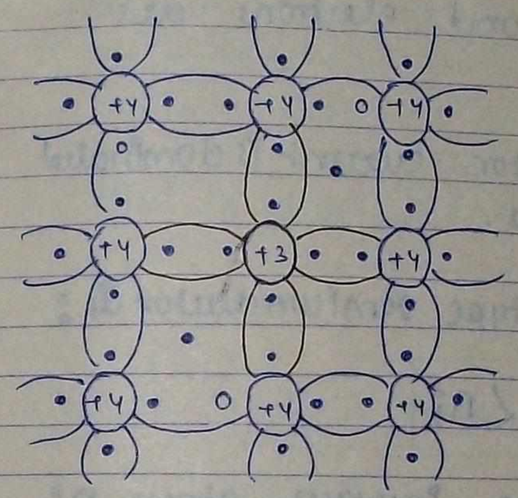
AT T=0k

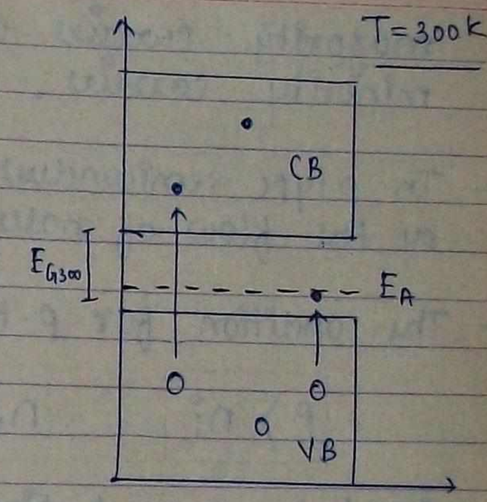


- Acceptor energy level denotes the energy level of trivalent atoms added to the pure semiconductor.

- P type semiconductor at 0 K will be working as an insulator.

AT T=300k





- In the p-type semiconductor, every impurity atom will be receiving one electron to complete its covalent bonding (hence p-type is also called acceptors).

- In p type semiconductor as temperature is increasing (0k to 300k), because of thermal energy a number of covalent bonds will be broken creating equal no. of electrons and holes. ~~Majority~~ most of the electrons will be moving from valence band into acceptor energy level to complete the bonding and a very few electrons will be moving from valence band into conduction band. The hole concentration in the valence band is far greater than electron concentration in the conduction band. Hence holes are

majority carrier and electrons are minority carrier.

- In p type semiconductor current is dominated by the flow of holes.

- The condition for p-type semiconductor is:

$$\boxed{p > n_i} \qquad \boxed{n < n_i}$$

- As hole concentration increases above n_i, the electron concentration falls below n_i and this is due to bonding.

- According the law of electrical neutrality

$$\boxed{N_D + p = N_A + n}$$

In p type semiconductor $N_D = 0$

$$\boxed{p = N_A + n} \quad \text{(exact eqn)}$$

also $p \gg n$

$$\boxed{p \simeq N_A}$$

- where N_A is called acceptor concentration and it denotes the no. of trivalent atoms added to the pure semiconductor.

$$\boxed{N_A = \text{TOTAL NO OF ATOMS}/cm^3 \times \text{IMPURITY RATIO}}$$

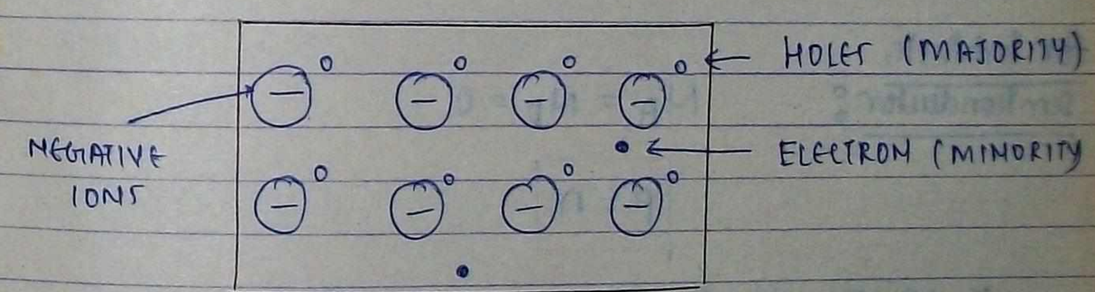
- The conductivity of p-type semiconductor is:

$$\boxed{\sigma_p = nq\mu_n + pq\mu_p} \quad \mho/cm$$

$$\boxed{\sigma_p \simeq pq\mu_p \simeq N_A q \mu_p} \quad \mho/cm.$$

- The conductivity due to minority carrier is almost negligible.

⇒ REPRESENTATION OF P-TYPE SEMICONDUCTOR –



- In p-type semiconductor the impurity atom will receiving the electron and gain a negative charge and become a negative ion.

- Negative ion means a neutral atom with one or more electron.

⇒ LAW OF ELECTRICAL NEUTRALITY –

It is based on the law of conservation of charge.

TOTAL POSITIVE CHARGE = TOTAL NEGATIVE CHARGE

$$\boxed{N_D + P = N_A + n}$$

or

$$\boxed{N_D - N_A = n - P}$$

– The semiconductor which will obey the law of electrical neutrality will be always electrically neutral.

for intrinsic semiconductor: $N_A = N_D = 0$

$$\boxed{P = n}$$

∴ Intrinsic semiconductor is electrically neutral

for n-type: $N_A = 0$

$$n = N_D + P$$

$$\boxed{n \simeq N_D}$$

for P-type: $N_D = 0$

$$P = N_A + n$$

$$\boxed{P \simeq N_A.}$$

– all semiconductors are electrically neutral.

Que. N type S.C. is ___.

(a) – ve charged
(b) + ve charged
(c) no charge at all
✓(d) Electrically neutral.

ANS. (D)

⇒ GERMANIUM & SILICON CRYSTAL –

⇒ GERMANIUM – SILICON CRYSTAL –

– The type of bonding is covalent bond

– At 0K they will behave as insulators.

– At 300K they will behave as intrinsic semiconductor.

Qu. A pure semicond^n (Ge) is doped with donar impurity to the extend of 1:10^7 calculate :

(1) donar conuntration
(2) conuntration of e^- and holes
(3) conductivity & resistivity of doped S.C.
(4) How many times the conductivity is increase due to doping.

Assume total no. of atom as $4.421 \times 10^{22}/cm^3$, $n_i = 2.5 \times 10^{13}$ atoms/cm^3, $\mu_n = 3800\ cm^2/Vsec$, $\mu_p = 1800\ cm^2/Vsec$.

Sol^n:

Because of donar impurity, the S.C. becomes n-type.

(1) N_D = total no of atoms/cm^3 × impurity ratio

$$= 4.421 \times 10^{22} \times \frac{1}{10^7}$$

$$= 4.421 \times 10^{15} \text{ atoms}/cm^3$$

(2) In n type semiconductor –

$$n \simeq N_D = 4.421 \times 10^{15} \text{ atoms}/cm^3$$

$$p = \frac{n_i^2}{N_D} = \frac{(2.25 \times 10^{13})^2}{4.421 \times 10^{15}} = 1.41 \times 10^{11}/cm^3$$

when S.C is intrinsic

$$n = p = n_i = 2.5 \times 10^{13}/cm^3$$

Due to donar conc.

$n \uparrow$ 10^{13} to $10^{15}/cm^3$

$p \downarrow$ 10^{13} to $10^{11}/cm^3$

$$n_n p_n = n_i^2$$

$$np \equiv n_n p_n \equiv n_i^2$$

(3) $\sigma_n = N_D \cdot q \cdot \mu_n$

$$= (4.421 \times 10^{15})(1.6 \times 10^{-19}) \times 3800$$

$$\simeq 2.68\ \mho/cm$$

$$\rho_n = \frac{1}{\sigma_n} = \frac{1}{2.68} = 0.373\ \Omega cm.$$

(4) Before doping S.C is intrinsic

$$\sigma_i = n_i q [\mu_n + \mu_p]$$

$$= 2.5 \times 10^{13} \times 1.6 \times 10^{-19} [3800 + 1800]$$

$$= 0.0224\ \mho/cm$$

By doping conductiving increase from 0.0224 ℧/cm to 2.68 ℧/cm.

∴ Increase in conductivity $= \frac{2.68}{0.0224} = 119.6 \simeq 120$ times.

Que. A pure S.C. (Si) is doped with acceptor impurities to the extent of 4 impurity atoms for every 10^6 atoms. Find its conductivity.
Assume total no. of atoms $5\times10^{22}/cm^3$
$n_i = 1.5\times10^{10}$ atoms/cm^3, $\mu_n = 1300\ cm^2/Vsec$
$\mu_p = 500\ cm^2/Vsec$

Soln:

$$N_A = 5\times10^{22}\times\frac{4}{10^6}$$
$$= 20\times10^{16}$$

$$\sigma \simeq p\,q\,\mu_p$$
$$\simeq 20\times10^{16}\times1.6\times10^{-19}\times500$$
$$\simeq 16\ ℧/cm$$

Que. A pure S.C (Si) is doped with donar impurity to extent of 1:10 6 calculate
(1) conductivity due to majority carrier
(2) conductivity due to minority carrier
Assume total no of atoms $5\times10^{22}/cm^3$
$n_i = 1.5\times10^{10}$ atom/cm^3, $\mu_n = 1300\ cm^2/Vsec$
$\mu_p = 500\ cm^2/Vsec$

Soln:

$$N_D = 5\times10^{22}\times\frac{1}{10^6} = 5\times10^{16}$$
$$n = N_D = 5\times10^{16}/cm^3$$
$$p = \frac{n_i^2}{N_D} = 3\times10^{-7}/cm^3\ (4500/cm^3)$$

(1) σ_n (majority) $= N_D\,q\,\mu_n$
$$= 5\times10^{16}\times1.6\times10^{-19}\times1300$$
$$= 10.4\ ℧/cm$$

(2) σ_p (minority) $= p\,q\,\mu_p$
$$= 3\times10^{-7}\times1.6\times10^{-19}\times500\times4500$$
$$= 3.6\times10^{-13}\ ℧/cm.$$

Que. In a S.C at room temp. the intrinsic conc. and intrinsic resistivity are $1.5\times10^{16}/m^3$ and $2\times10^3\ \Omega m$ resp. It is converted into extrinsic semicondn with a doping conc. of $10^{20}/m^3$. for the extrinsic S.C. calculate

(1) minority carrier conc.
(2) electron mobility
(3) resistivity of the doped S.C.
(4) minority carrier conc. when its temp is increased to a value when intrinsic conc. n_i is double.

Assume the mobility of magority carrier is equal to the mobility of minority carrier.

Sol^n: $\mu_n \equiv \mu_p$

$n_i = 1.5 \times 10^{16} / m^3$ $\rho_i = 2 \times 10^3 \Omega m$

doping con. $= 10^{20} / m^3$

(1) $\frac{\text{minority}}{\text{carrier}} = \frac{n_i^2}{10^{20}} = \frac{n_i^2}{\text{Doping conc.}}$

$= 2.25 \times 10^{12} / m^3$

(2) $\frac{1}{2 \times 10^3} = 2.25 \times 10^{12} \times 1.6 \times 10^{-19} \times \mu_A$

$\mu_A = \mu_p = \mu$

$\rho_i = \frac{1}{n_i q (\mu_n + \mu_p)}$

$\mu = \frac{1}{\rho_i n_i 2 . q}$

$= \frac{1}{2 \times 10^3 \times 1.5 \times 10^{16} \times 2 \times 1.6 \times 10^{-19}}$

$= 0.1042 \ m^2/V sec.$

(3) $\rho_{doped} = \frac{1}{\sigma_{doped}}$

$= \frac{1}{\text{carrier con} \times q \times \mu}$

$= \frac{1}{10^{20} \times 1.6 \times 10^{-19} \times 0.1042}$

$= 0.5998 \ \Omega m$

(4) as temp ↑ n_i get doubled

new n_i is $n_i' = 2 n_i$

$n_i' = 2 \times 1.5 \times 10^{16}$ atom/m^3

minority carrier con. with ↑ temp $= \frac{(2 \times 1.5 \times 10^{16})^2}{20}$

$= 9 \times 10^{12} / m^3$

(*)

Qu. A Si s.c. is doped with donor impurity with resultant doping profile as $n = Gx$ and $n \gg n_i$, the sample is placed isolated. find built in electric field as an funⁿ. of x., also calculate the field at $x = 1\ \mu m$

Solⁿ:

(1) $J_n = J_n(\text{drift}) + J_n(\text{diff})$

$$J_n = nq\mu_n \mathcal{E} + qD_n \frac{dn}{dx} \quad -(1)$$

Since sample is isolated, $\boxed{J_n = 0}$

$n = Gx$ (given)

$$\frac{dn}{dx} = G$$

from (1) $0 = Gx\, q\mu_n \mathcal{E} + qD_n G$

$$x\mu_n \mathcal{E} = -D_n$$

$$\mathcal{E} = \frac{-D_n}{\mu_n x}$$

but $\frac{D_n}{\mu_n} = V_T$

$$\boxed{\mathcal{E} = -\frac{V_T}{x}}$$

Built in electric field in s.c. as a function of x.

(1) $x = 1\ \mu m$ $V_T = 26\ mV$ at room temp.

$$\mathcal{E} = \frac{-V_T}{x} = \frac{-26 \times 10^{-3} V}{1 \times 10^{-6} m}$$

$$\mathcal{E} = -26\ kV/m$$

Qu. find conductivity and resistivity of pure Ge at room temp..

Assume $n_i = 2.5 \times 10^{13}$ atoms/cm³, $\mu_n = 1300\ cm^2/Vsec$, $\mu_p = 1800\ cm^2/V\text{-}sec$.

Solⁿ:

$$\sigma_i = n_i q [\mu_n + \mu_p]$$

$$= 2.5 \times 10^{13} \times 1.6 \times 10^{-19} [1300 + 1800]$$

$$= 0.0224\ \mho/cm.$$

$$\rho_i = \frac{1}{\sigma_i} = 44.6\ \Omega cm$$

Qu. find intrinsic conductivity & intrinsic resistivity for silicon at 300k.

$n_i = 1.5 \times 10^{10}$ atom/cm³, $\mu_n = 1300\ cm^2/Vsec$

$\mu_p = 500\ cm^2/Vsec$.

Solⁿ:

$$\sigma_i = n_i q [\mu_n + \mu_p]$$

$$= 4.32 \times 10^{-6}\ \mho/cm$$

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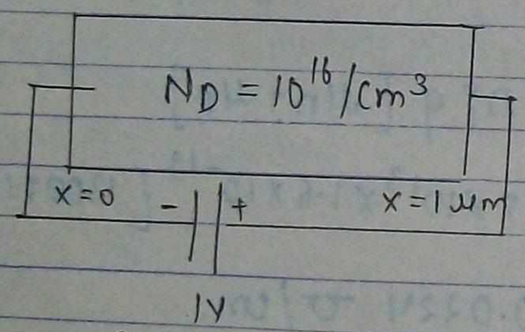
$$\rho_i = \frac{1}{\sigma_i} = \frac{1}{4.32 \times 10^{-6}}$$

$$= \underline{\underline{231,481}} \ \Omega\,cm$$

Que. The Si sample with unit crosssectional area given below is under thermal equilibrium the following information is given:
$T = 300k$, $q = 1.6 \times 10^{-19} C$, $V_T = 26 mV$
$\mu_n = 1350 \ cm^2/Vsec$.



(1) The magnitude of the electric field at 0.5 μm is. ___
(A) 1 kV/cm (B) 5 kV/cm (C) 10 kV/cm
(D) 26 kV/cm

(2) The magnitude of the electron drift current density at $x = 0.5$ μm. is ___.
(A) 2.16×10^4 A/cm² (B) 1.08×10^4 A/cm²
(C) 4.32×10^3 A/cm² (D) 6.48×10^2 A/cm²

Soln: $N_D = 10^{16}/cm^3$

(1) $\mu = V/\mathcal{E}$

$$|\mathcal{E}|_{x=0.5} = \frac{|V_c|}{X_c} = \frac{0.5V}{0.5 \times 10^{-6} m}$$

$$= 10^6 V/m \quad \text{or } 10^4 V/cm.$$

(2) $J_{n(DIFF)} = nq\mu_n |\mathcal{E}|_{x=0.5}$

$$= 10^{16} \times 1.6 \times 10^{-19} \times 1350 \times 10^4$$

$$= 2.16 \times 10^4 \ A/cm^2.$$

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⇒ MINIMUM VALUE OF CONDUCTIVITY IN S.C –

The general eqⁿ for conductivity in a semiconductor is given by.

$$\sigma = nq\mu_n + pq\mu_p \quad -(1)$$

By mass action law, $p = \frac{n_i^2}{n}$ – (2)

Substituting eq (2) in eq (1):

$$\sigma = nq\mu_n + \frac{n_i^2}{n} \cdot q\mu_p$$

Differentiating above eqⁿ wrt n:

$$\frac{d\sigma}{dn} = q\mu_n - \frac{n_i^2}{n^2} q\mu_p$$

$$\frac{d^2\sigma}{dn^2} = \left(\frac{2}{n^3}\right) n_i^2 q\mu_p.$$

Since second derivative is positive we get the condition for minimum conductivity in the semiconductor.

The eqn for minimum conductivity can be obtain by equating $\frac{d\sigma}{dn} = 0$.

$$q\mu_n - \frac{n_i^2}{n^2} q\mu_p = 0$$

$$\mu_n = \frac{n_i^2}{n^2} \cdot \mu_p$$

$$\boxed{n = n_i \sqrt{\frac{\mu_p}{\mu_n}}} \quad – (A)$$

Eq (A) denotes the conc. of electrons in the semiconductor when conductivity is minimum.

Eq (A) also indicates thermal equilibrim electrons.

If the semiconductor is p-type and thermal equilibrim e^- is denoted by n_0

$$\boxed{n_0 = n_i \sqrt{\frac{\mu_p}{\mu_n}}}$$

Substituting eq (A) in eq (2):

$$p = \frac{n_i^2}{n_i \sqrt{\frac{\mu_p}{\mu_n}}} = n_i \sqrt{\frac{\mu_n}{\mu_p}}$$

$$\boxed{p = n_i \sqrt{\frac{\mu_n}{\mu_p}}} \quad – (B)$$

eq (B) denotes the conc. of holes in the semiconductor when the conductivity is minimum.

eq (B) also indicates the Thermal equilibrium holes, if the S.C. is n-type and is denoted by P_0

$$\boxed{P_0 = n_i \sqrt{\frac{\mu_n}{\mu_p}}}$$

Substituting eq (A) and (B) in eq (1): we get the condi equation for min. conductivity.

$$\sigma = n_i \sqrt{\frac{\mu_p}{\mu_n}}\, q\mu_n + n_i \sqrt{\frac{\mu_n}{\mu_p}}\, q\mu_p$$

$$\sigma_{min} = n_i q \left[\sqrt{\mu_n \mu_p} + \sqrt{\mu_p \mu_n} \right]$$

(A) $$\boxed{\sigma_{min} = 2 q n_i \sqrt{\mu_n . \mu_p}}$$

Que. A S.C. have following parameters
$\mu_n = 7500\ cm^2/V\,sec$, $\mu_p = 300\ cm^2/V\,sec$
$n_i = 3.6 \times 10^{12}/cm^3$, find
(1) min. σ
(2) Hole conc. in the S.C when σ is min.
(3) Thermal equilibrium e^- in the S.C.

Soln:

(1) $$\sigma_{min} = 2 q n_i \sqrt{\mu_n \mu_p}$$

$$= 2 \times 1.6 \times 10^{-19} \times 3.6 \times 10^{12} \times \sqrt{7500 \times 300}$$

$$= 1.7 \times 10^{-3}\ \mho/cm$$

(2) $$P_0 = n_i \sqrt{\frac{\mu_n}{\mu_p}}$$

$$= (3.6 \times 10^{12}) \times \sqrt{\frac{7500}{300}}$$

$$= 1.8 \times 10^{13}/cm^3$$

(3) $$n_0 = n_i \sqrt{\frac{\mu_p}{\mu_n}}$$

$$= (3.6 \times 10^{12}) \times \sqrt{\frac{300}{7500}}$$

$$= 7.2 \times 10^{11}/cm^3$$

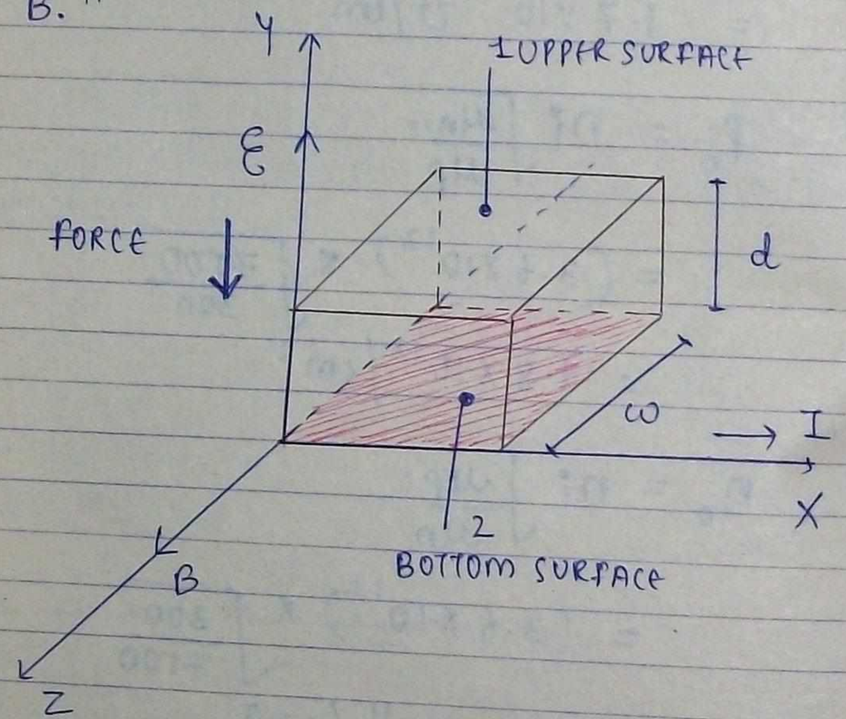
Ans. (1) $1.7 \times 10^{-3}\ \mho/cm$

(2) $1.8 \times 10^{13}/cm^3$

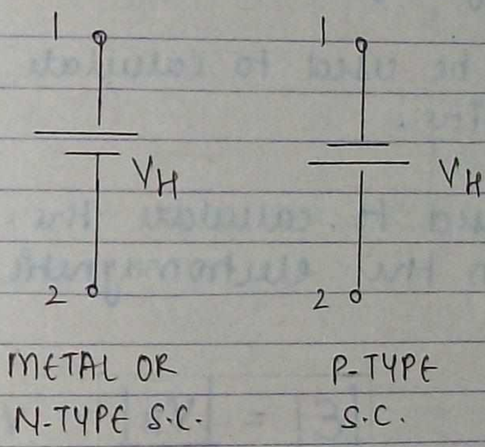
(3) $7.2 \times 10^{11}/cm^3$

⇒ HALL'S EFFECT –

Hall effect states that "If a specimen (metal or semiconductor) carrying a current I is placed in a transverse magnetic field B, then an electric field E is induced in a direction perpendicular to both I and B."



- The specimen must be square or rectangle in shape.
- current direction is taken on x direction, magnetic field is taken on z direction and electric field in the y direction
- w is width of the specimen, d is the height or thickness of the specimen and it is also the spacing between the bottom surface and upper surface of the specimen.



- The polarity and magnitude of the induced hall voltage will indicate, whether it is a metal or semiconductor
- Hall voltage is induced voltage.
- By using hall experiment:

1. we can determine whether the given specimen is a metal or a semiconductor.
2. we can find concentration of charge carriers.

3. we can calculate mobility of charge carriers.

4. HALL experiment can be used in designing of HALL EFFECT transducers.

5. It can be used to calculate magnetic flux density.

6. Can be used to calculate the signal power in the electromagnetic waves.

Electric field intensity,

$$\boxed{|\mathcal{E}| = \frac{|V_H|}{d}} \quad V/m$$

∴ Hall voltage

$$\boxed{V_H = \mathcal{E}.d} \quad \text{volts}$$

also.

$$\boxed{V_H = \frac{BI}{\rho w}} \quad \text{volts.}$$

where ρ = charge density.

and $\frac{1}{\rho} = R_H$ = hall coefficient

$$\boxed{V_H = \frac{BI.R_H}{w}} \quad \text{volts.}$$

$$\boxed{V_H \propto R_H}$$

- In hall experiment

$$\boxed{\mu = \frac{8}{3\pi}\sigma R_H}$$

$$\boxed{\mu \simeq \sigma R_H}$$

where, σ is called conductivity of the specimen.

APPLICATIONS -

1. Magneto field meter.
2. Hall effect multiplier.

NOTE -

- Magneto field meter is an instrument used to measure magnetic flux density B (weber/m^2)

- form the hall experiment we can measure magnetic field intensity (H).

$$\boxed{H \propto B}$$

- Charge density ρ ;

$$\boxed{\rho = \text{charge} \times \text{carrier concentration}} \quad C/m^3$$

- Hall coefficient R_H :

$$R_H = \frac{1}{\rho}$$

$$\boxed{R_H = \frac{1}{\text{CHARGE} \times \text{CARRIER CONC.}}} \quad m^3/C$$

- If one input signal is applied in the form of current and another input signal is applied in the form of magnetic field (B), then induced hall voltage is directly proportional to the product of the two I/P signals. Hence hall experiment can be used in designing of hall effect multiplier

$$\boxed{V_H = \frac{BI}{\rho w}}$$

Induced hall voltage is directly prop. to multiplication of the two I/P signal <u>B and I</u>

If the polarity of hall voltage is +ve for the bottom surface then the given specimen — <u>P-TYPE SEMICONDUCTOR.</u>

- Hall voltage is measured with reference to bottom surface

- for metals hall voltage is negative, for N-type semiconductor hall voltage is negative, for P-type semiconductor is positive.

- for intrinsic semiconductor hall voltage is zero.

- In the hall experiment :

$$\mu \simeq \sigma R_H$$

$$R_H \simeq \frac{\mu}{\sigma}$$

Since $V_H \propto R_H$

$$\boxed{V_H \propto \frac{1}{\sigma}}$$

- <u>IN METALS</u> — conductivity is very large V_H is small (μV)

- IN S.C -

Conductivity is small, hence V_H is large (mV).

Que. Hall voltage is small in ____.
Hall voltage is large in ____.

Soln: (A) METALS (B). SEMICONDUCTOR.

- The mobility of charge carriers can be experimentally found by using hall effect.

- The mobility of charge carriers can also be experimentally found by using HAYNEES - SCHOCKLEY experiment.

- Haynes - schockley experiment can be used to determine:

1. mobility of charge carriers.

2. Diffusion constant of the charge carriers ($D = \mu V_T$, $D \propto \mu$)

Que. A doped S.C. specimen has hall coefficient 3.6×10^{-4} m^3/C and resistivity 9×10^{-3} Ωm assuming single carrier conduction, the mobility and density of carriers in the specimen approximately given by —.

Soln: (1) $R_H = 3.6 \times 10^{-4}$ m^3/C

$\rho = 9 \times 10^{-3}$ Ωm
resistivity

$$\sigma = \frac{1}{\rho} = 0.11 \times 10^{-3}$$

$$\mu \cong \sigma R_H \cong (0.11 \times 10^{-3})(3.6 \times 10^{-4})$$

$$\cong \underline{\underline{0.4}}$$

(2) $$R_H = \frac{1}{\text{charge} \times \text{carrier con.}}$$

$$\text{carrier conc.} = \frac{1}{q R_H} = \frac{1}{1.6 \times 10^{-19} \times 3.6 \times 10^{-4}}$$

$$= 1.736 \times 10^{22} / m^3$$

OR

assuming single carrier conduction.

$$\text{Conductivity} = \text{carrier conc.} \times q \times \mu$$

$$\text{Carrier con.} = \frac{\text{conductivity}}{q\mu} = \frac{1}{\text{Resistivity} \times q \mu}$$

$$= \frac{1}{9 \times 10^{-3} \times 1.6 \times 10^{-19} \times 0.04} = 1.736 \times 10^{22} / m^3$$

Qu. find the magnetic field in a rectangle S.C. specimen having 4 mm wide and 2 mm thick with a Hall coefficient of $10^{-3}\ m^3/C$ when a current of 1 mA is passing to the sample, a hall voltage of 2 mV is obtain.

Soln:

$$V_H = \frac{B \cdot I \cdot R_H}{w}$$

$$B = \frac{V_H \times w}{I \times R_H}$$

$$B = \frac{(2\times10^{-3})(4\times10^{-3})}{(1\times10^{-3})(10^{-3})}$$

$$B = 8\ wb/m^2.$$

Qu. find the magnitude of the hall coefficient in the N-type Ge bar having a width of 3 mm and height 2 mm assume $B = 0.9\ wb/m^2$, $E = 5\ V/cm$, $I = 1.5\ mA$.

Soln:

$$V_H = \frac{B \cdot I \cdot R_H}{w}$$

$$R_H = \frac{V_H \cdot w}{B \cdot I}$$

$$V_H = Ed$$

$$= 5 \times 2\times10^{-3} = 10\times10^{-3}\ V$$

$$R_H = \frac{(10\times10^{-3}) \times (3\times10^{-3})}{(0.9) \times (1.5\times10^{-3})}$$

$$R_H = 2.22\ m^3/C.$$

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Qu. A n type Ge sample is 2 mm wide & 0.2 mm thick, a current of 10 mA is passed through the sample (x-direction) and a magnetic field of $0.1\ wb/m^2$ is directed perpendicular to the current flow (z-direction), the developed hall voltage is $-1.0\ mV$. Calculate the hall coefficient and electron concentration.

Soln:

(1) $$R_H = \frac{|V_H| \cdot w}{B \cdot I}$$

$$= \frac{(+1.0\times10^{-3})(2\times10^{-3})}{(0.1) \times (10\times10^{-3})}$$

$$= 2\times10^{-3}\ m^3/C$$

(2) $$e^- \text{ conc.} = n \simeq \frac{1}{qR_H}$$

$$= \frac{1}{1.6\times10^{-19} \times 2\times10^{-3}} = 312.5\times10^{19}/m^3$$

⇒ CARRIER CONCENTRATION IN INTRINSIC S.C. –

- In intrinsic semiconductor, carrier conc. means, electron conc. and hole conc.

- Effect of temperature on carrier conc. in intrinsic S.C.

EFFECT OF TEMP.

$$n = p = n_i$$

but $n_i \propto T^{3/2}$

$\therefore$ $n \uparrow$ and $p \uparrow$ with Temp.

- In intrinsic semiconductor carrier conc. increases with the temperature.

⇒ EFFECT OF TEMP. ON CONDUCTIVITY OF INTRINSIC SEMICONDUCTOR –

$$\sigma_i = n_i q [\mu_n + \mu_p]$$

$\sigma_i \propto n_i$ and $n_i \propto T^{3/2}$

$\therefore$ $\sigma_i \uparrow$ with Temp.

- In intrinsic S.C conductivity increases with temperature.

⇒ CARRIER CONC. IN EXTRINSIC SEMICONDUCTOR –

- In extrinsic semiconductor, carrier conc. means majority carrier conc.

⇒ EFFECT OF DOPING ON CARRIER CONC. IN EXTRINSIC S.C. –

FOR N-TYPE S.C.	FOR P-TYPE S.C.
$n \simeq N_D$	$p \simeq N_A$

- In extrinsic semiconductor carrier conc. increases with doping.

⇒ EFFECT OF DOPING ON MAJORITY & MINORITY CARRIERS –

	N-TYPE S.C.	P-TYPE S.C.
majority carrier	$n \simeq N_D$	$p \simeq N_A$
minority carrier	$p \simeq \frac{n_i^2}{N_D}$	$n \simeq \frac{n_i^2}{N_A}$

$$\boxed{\text{MAJORITY CARRIER CONC.} \propto \text{DOPING}}$$

$$\boxed{\text{MINORITY CARRIER CONC.} \propto \frac{1}{\text{DOPING}}}$$

- Doping increases majority carriers but doping reduces minority carriers

⇒ **EFFECT OF DOPING ON THE CONDUCTIVITY OF EXTRINSIC S.C. –**

N - TYPE	P - TYPE
$\sigma_N \simeq N_D q \mu_n$	$\sigma_P \simeq N_A q \mu_p$
$\sigma_N \propto N_D$	$\sigma_P \propto N_A$

- Doping increases the conductivity of the extrinsic semiconductor.

- A highly doped s.c. will exhibit metallic properties i.e. conductivity will become very large, the semiconductor can become unipolar, NTC of resistance will be converted into PTC of resistance

NOTE –

A highly doped semiconductor behaves as a metal.

⇒ **EFFECT OF TEMP. ON MAJORITY & MINORITY CARRIERS –**

Consider a Si bar subjected to donor impurity of $1:10^6$

$$N_D = 5 \times 10^{22} \times \frac{1}{10^6}$$

$$N_D = 5 \times 10^{16} \text{ atoms/cm}^3$$

thus semicond^n becomes N-type and in N type S.C –

$$n \simeq N_D \simeq 5 \times 10^{16} \text{ atom/cm}^3$$

$$p \simeq \frac{n_i^2}{N_D} = 4500/\text{cm}^3$$

let temperature increases and let 10^6 covalent bond are broken.

Thermally generated $e^- = 10^6/\text{cm}^3$

Thermally generated $p = 10^6/\text{cm}^3$

Total no. of e^- in C.B. $= 5 \times 10^{16} + 10^6 \simeq \underline{\underline{5 \times 10^{16}/\text{cm}^3}}$

Total no of holes in V.B $= 4500 + 10^6 \simeq \underline{\underline{10^6/\text{cm}^3}}$

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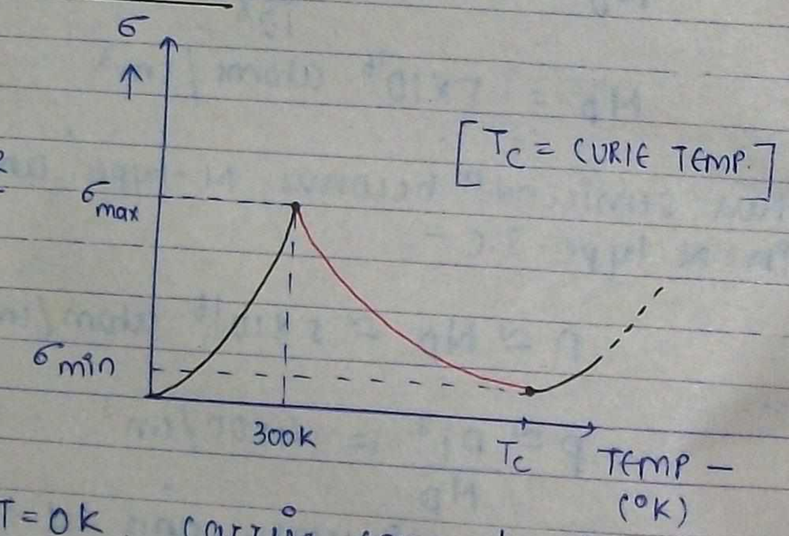
- majority carrier conc. is almost independent of temp.

- minority carrier conc. increases with the temp.

⇒ **EFFECT OF TEMP. ON CONDUCTIVITY OF EXTRINSIC S.C. –**

σ Vs T CURVE FOR EXT. S.C.



- AT, T=0K, carrier concentration are zero and therefore the extrinsic S.C. will behave as intrinsic S.C. as insulator.

- when 0K < T < 300K, as temperature is increasing, majority and minority carrier are created and the conductivity increases with the temperature.

- AT T=300K, the conductivity of extrinsic S.C. is maximum.

- AT 300K < T < T_c, as temperature is increasing above 300K, mobility of charge carriers decreases and therefore the conductivity of extrinsic S.C. decreases.
  As temperature is increasing majority carrier conc. will remain almost a constant.
  As temp. is increasing the minority carrier conc. will be increasing with the temperature.

- At T = T_c (curie temp), the conductivity of extrinsic S.C. will be reduced to minimum conductivity.
  At curie temp minority carrier conc. approaches majority carrier concentration and therefore the extrinsic S.C. will become intrinsic S.C., but conductivity is slightly greater than conductivity of intrinsic S.C.

- ABOVE T_c, as temperature is increasing the conductivity of the S.C. will be now increasing with the temp. (because the extrinsic S.C. has now become intrinsic)

- At very high temperature, extrinsic S.C is intrinsic semiconductor.

- At very low temps. the conductivity of extrinsic S.C increases with the temp.

- At curie temp. extrinsic S.C. becomes intrinsic S.C. and the purpose of doping the S.C. is lost

- In extrinsic S.C. as temperature increase the conductivity decrease.

NOTE -

INTRINSIC S.C	EXTRINSIC S.C.
(1) $\sigma \uparrow$ with T.	(1) $\sigma \downarrow$ with T
(2) $\rho \downarrow$ with T.	(2) $\rho \uparrow$ with T.

⇒ CLASSIFICATION OF SEMICONDUCTORS -

SEMICONDUCTOR

- DIRECT BAND GAP. S.C (DBG)
- INDIRECT BAND GAP. S.C. (IBG

DBG - SC	IBG - SC
1. During the recombination most of the energy is dissipated in the form of LIGHT.	1. During recombination most of the energy is dissipated in the form of HEAT.
Ex - GaAs ✓ (IES) GaN, GaSb, InAs, ZnS, ZnSe, CdS, CdSe, InP	Ex - Si ✓ & Ge ✓ (IES) AlP, AlSb, PbS, PbSe, GaP.
2. During recombinations, most of the falling e^- from C.B. will be directly falling into V.B. and they release the energy in the form of light, but very few falling e^- from the C.B. will be colliding with the crystals of the atom and these crystall will absorb the energy from the falling e^- & gets heated up and these crystal will be now relasing the energy in the form of heat	2. During recombination most of the falling e^- from C.B will be colliding with the crystals of the atom and these crystal will absorb the energy from the falling e^- & gets heated up & they will be relasing the energy in the form of heat But, very few falling e^- will be escaping the collision & will be directly falling into V.B. & release energy

(momentum = mass × velocity)

(99% LIGHT and 1% HEAT)	in the form of Light (99% HEAT & 1% LIGHT)
3. most of the falling e^- from the C.B will be directly releasing the energy in the form of light and the name DIRECT BAND GAP S.C.	3. most of the falling e^- will be indirectly releasing the energy, through the crystal of atom and become heated in the form of heat and hence the name INDIRECT BAND GAP S.C.
4. The energy of the falling e^- changes (both KE & PE changes)	4. The energy of the falling e^- changes (both KE & PE changes)
5. The direction of the falling e^- is unaffected	5. The direction & the path of the e^- slightly changes because of collisons.
6. The momentum of the falling e^- changes	6. The momentum of the falling e^- changes.
7. Relatively carrier life-time is small.	7. Relatively carrier life time is large.

* Si is not used in - LED

*

Que. Si is never used in the fabrication of LEDs because it is ____ semiconductor.

Soln: INDIRECT BAND GAP S.C.

* Silicon cannot be used in the fabrication of:

LEDs, LASER, TUNNEL DIODES, VARACTOR DIODE, PIN DIODE, GUN DIODE.

Que. S.C. Lasers are fabricated with direct band gap S.C. having large carrier life time.

Soln: carrier life time is large.

Que. GaAs is an example for

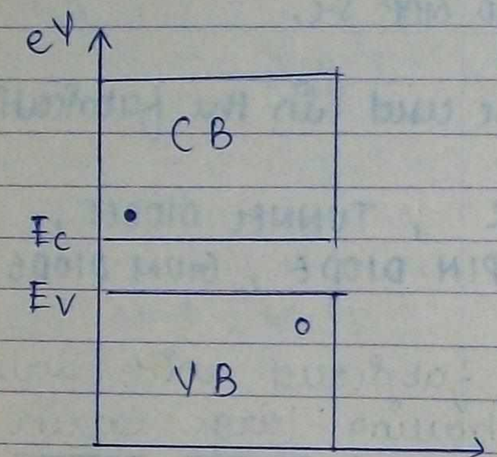
(A) DBG S.C
(B) IBG S.C
(C) WIDE BAND GAP S.C
(D) NARROW BAND GAP S.C.

of these the correct statement are:

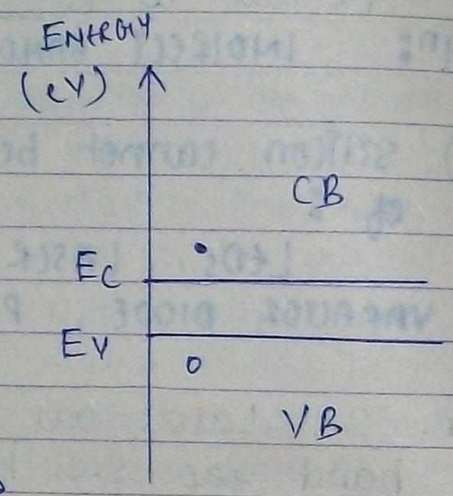
1. only D
2. only A
3. A and C
4. B and C.

Ans. 2, wide band & narrow band gap S.C does not exist.

⇒ EQUATION FOR CONCENTRATION OF ELECTRONS IN THE CONDUCTION BAND -



APPROXIMATE ENERGY BAND DIAGRAM



EXACT ENERGY LEVEL DIAGRAM.

- E_V maximum energy of the valence band
- E_C minimum energy of the conduction band
- The energy possessed by a free e^- in the conduction band varies from E_C to $+\infty$.
- The concentration of e^- in the conduction band is given by

$$\boxed{n = N_C\, e^{-[E_C - E_F]/KT}}$$

E_F = fermi energy in eV.

N_C = material constant and is a function of temperature.

$$N_C = 2\left[\frac{2\pi \bar{k} T m_n}{h^2}\right]^{3/2}$$

$$\boxed{N_C = 2\left[\frac{2\pi \bar{k} m_n}{h^2}\right]^{3/2} \cdot T^{3/2}}$$

- N_C is approximatly equal to the density of states in the conduction band.

h = planks constant.

m_n = effective mass of the electron.

$m_n < m$

m → Rest mass of e^-. (9.1×10^{-31} kg)

- Effective mass of the e^- indicates mass of the electron when the e^- is revolving.
- Effective mass of the e^- depends on the type of material.

⇒ CONCENTRATION OF HOLES IN VALANCE BAND -

- Energy possessed by holes in the valence band is from $-\infty$ to E_V

- concentration of holes in valence band is :

$$\boxed{P = N_V e^{-[E_f - E_V]/kT}}$$

- N_V is a material constant and it is a function of temperature.

$$N_V = 2\left[\frac{2\pi \bar{k} T m_p}{h^2}\right]^{3/2}$$

$$\boxed{N_V = 2\left[\frac{2\pi \bar{k} m_p}{h^2}\right]^{3/2} T^{3/2}}$$

m_p = Effective mass of hole

$= 1.6 \times 10^{-27}$ kg.

$m_n < m_p$

- N_V is approximately equal to the density of states in the valency band

- DERIVE AN EQUATION FOR INTRINSIC CONCENTRATION

$$n = N_C e^{-[E_C - E_f]/kT} \quad \text{— (1)}$$

$$p = N_V e^{-[E_f - E_V]/kT} \quad \text{— (2)}$$

multipling (1) and (2) :

$$np = N_C N_V e^{-[E_C - E_V]/kT}$$

let $E_C - E_V = E_G$ and $np = n_i^2$

$$n_i^2 = N_C N_V e^{-E_G/kT} \quad \text{— (3)}$$

$$N_C = 2\left[\frac{2\pi \bar{k} . m_n}{h^2}\right]^{3/2} . T^{3/2}$$

$$N_V = 2\left[\frac{2\pi \bar{k} m_p}{h^2}\right]^{3/2} . T^{3/2}$$

Substituting N_C, N_V values in eq (3) :

$$n_i^2 = 4\left[\frac{2\pi \bar{k} m_n}{h^2}\right]^{3/2}\left[\frac{2\pi \bar{k} m_p}{h^2}\right]^{3/2} . T^3 . e^{-E_G/kT}$$

thus,

$$n_i^2 = 4\left(\frac{2\pi k}{h^2}\right)^3 (m_n m_p)^{3/2} T^3 e^{-E_G/kT}$$

$$\boxed{n_i^2 = A_0 T^3 e^{-E_G/kT}}$$

where,

$$\boxed{A_0 = 4\left(\frac{2\pi k}{h^2}\right)^3 (m_n m_p)^{3/2}}$$

⇒ FERMI-ENERGY (E_F) –

- fermi energy is measured in eV.
- fermi energy is defined as the maximum energy possesed by the electron at 0°K.
- fermi energy is defined as the maximum kinetic energy possesed by the electron at 0K.

max. KE = E_F

$$E_F = \frac{1}{2} m v^2$$

max velocity of e^-
or
velocity of e^-

$$\boxed{v = \sqrt{\frac{2E_F}{m}}} \quad m/sec.$$

- fermi-energy is also defined as the energy possesed by fastest moving electron at 0K.

⇒ FERMI-DIRAC FUNCTION [f(E)] –

- It is also called fermi dirac probability function.
- for a metal or a semiconductor:

$$\boxed{f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}}$$

- E is the energy possesed by e^- expressed in eV.
- At T=0K, we get two condition:

(1) If $E > E_F$:

$$f(E) = \frac{1}{1+e^{\infty}} = 0 \quad , \quad \boxed{f(E) = 0}$$

(*) At 0K no electrons are available with energies $E > E_F$

② If $E < E_f$:

$$f(E) = \frac{1}{1+e^{-\infty}} = 1, \quad \boxed{f(E) = 1} \quad (\text{or } 100\%)$$

⊛ Above indicates at 0K some electrons are available with energies $E < E_f$.

- AT $T \neq 0K$,

If $E = E_f$.

$$f(E) = \frac{1}{1+e^{0}} = 1/2 \quad \boxed{f(E) = 0.5} \quad (50\%)$$

- fermi energy is the energy level with 50% probability of being filled if no forbidden band exists.

- fermi energy denotes the exis probability of electron existing as a function of $f(E)$

- for metals : $f(E) = 1$ (or 100%)

- In a semiconductor, if the probability of an electron existing is $f(E)$, then the probability of hole existing is given by :

$$= 1 - f(E)$$

⇒ FERMI LEVEL IN INTRINSIC SEMICONDUCTOR -

- In intrinsic semiconductor,

$$n = p$$

$$n = N_c e^{-(E_c - E_f)/kT}$$

$$p = N_v e^{-(E_f - E_v)/kT}$$

$$\therefore N_c e^{-(E_c - E_f)/kT} = N_v e^{-(E_f - E_v)/kT}$$

$$\frac{N_c}{N_v} = e^{(E_c + E_v - 2E_f)/kT}$$

$$\log \frac{N_c}{N_v} = \frac{E_c + E_v - 2E_f}{kT}$$

$$-2E_f + E_c + E_v = kT \log\left(\frac{N_c}{N_v}\right)$$

⊛ $$\boxed{E_f = \frac{E_c + E_v}{2} - kT \log_e\left(\frac{N_c}{N_v}\right)}$$

- In intrinsic S.C. fermi level depends only on temperature.

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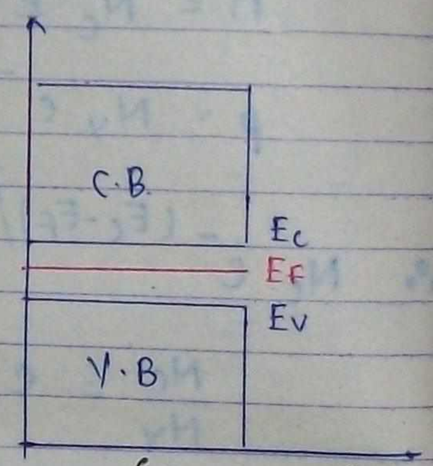
CASE ①: let $m_n = m_p$

$$N_c = N_v$$

$$\therefore \log_e\left(\frac{N_c}{N_v}\right) = 0$$

$$\boxed{E_F = \frac{E_c + E_v}{2}}$$

The fermi level is now existing at the middle or centre of the energy gap.



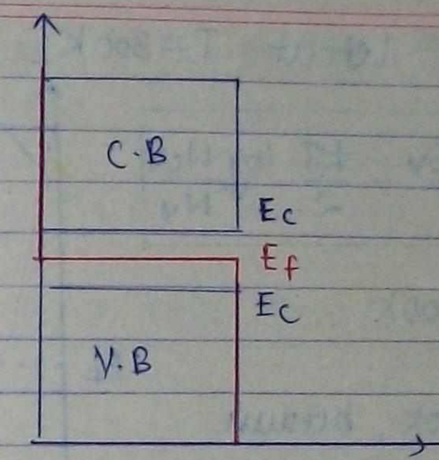
(AT T=0K)

CASE ②: If T=0

$$\boxed{E_f = \frac{E_c + E_v}{2}}$$

At T=0K, in intrinsic S.C. fermi level is existing at the centre of middle of the energy gap.

Diagram for fermi level at t=0k



(AT T=0K)

- at zero k carrier concentrations are zero and therefore conductivity is zero hence intrinsic S.C will be working as an insulator.

NOTE -

In intrinsic S.C. fermi level will be exisiting exactly at the centre of energy gap only when:

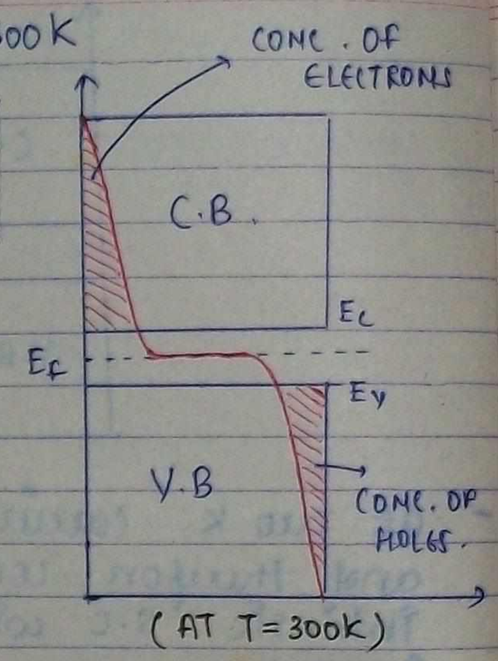
1. $m_n = m_p$ ✓
2. $N_c = N_v$ ✓
3. $T = 0K$ ✓

$$E_f = \frac{E_c + E_v}{2} \quad \text{(middle)}$$

CASE (3): Let at T = 300K

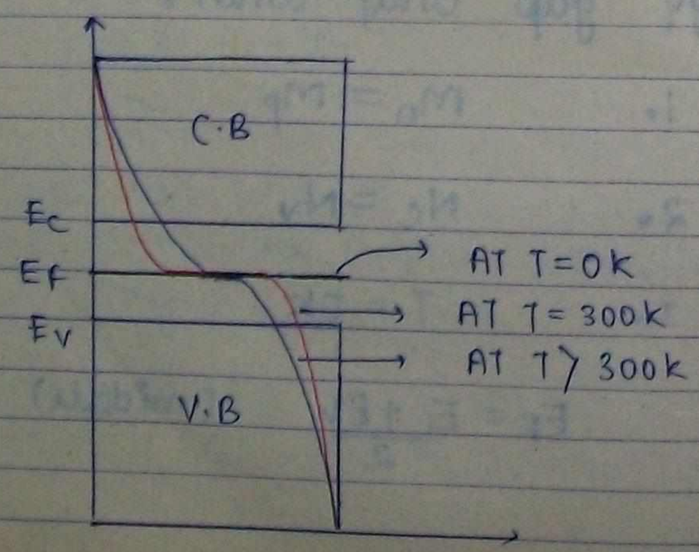
$$E_f = \frac{E_c + E_v}{2} - \frac{KT}{2} \log \frac{N_c}{N_v}$$

where T = 300K



At t = 300K, because of thermal energy a number of covalent bonds will be broken creating equal no. of electrons and holes & therefore there will be a conductivity in the S.C.

CASE (4): fermi-level at different temperatures.



- As temperature is increasing electron conc. and hole conc. increases and there by the conductivity of the intrinsic S.C. will be increasing with the temp.

⇒ FERMI LEVEL IN N-TYPE SEMICONDUCTOR –

$$n \simeq N_D$$

$$N_c e^{-(E_c - E_f)/KT} \simeq N_D$$

$$\frac{N_c}{N_D} = e^{(E_c - E_f)/KT}$$

$$E_c - E_f = KT \log_e\left(\frac{N_c}{N_D}\right)$$

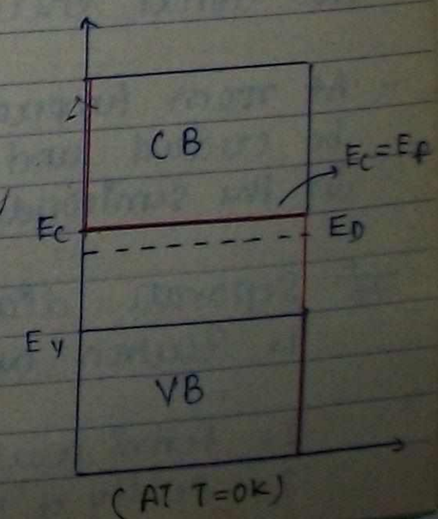
$$E_f = E_c - KT \log_e\left(\frac{N_c}{N_D}\right)$$

- In N-type S.C. fermi level function of temp and doping concentration.

CASE (1): let T = 0K

$E_f = E_c$

↓



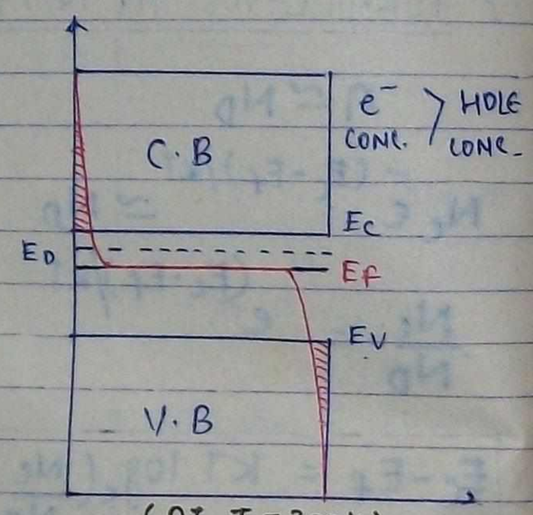
mean E_f coincides with E_c.

- At T=0K carrier conc. are zero hence conductivity is zero, N-type S.C at zero kelvin will be working as an insulator.

CASE (2): AT T=300K

$$E_f = E_c - kT \log_e\left(\frac{N_c}{N_D}\right)$$

where T=300K and N_c value must be for 300K.

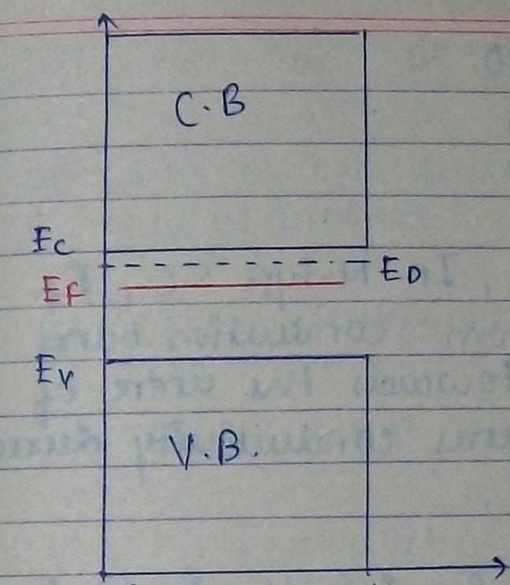


(AT T=300K)

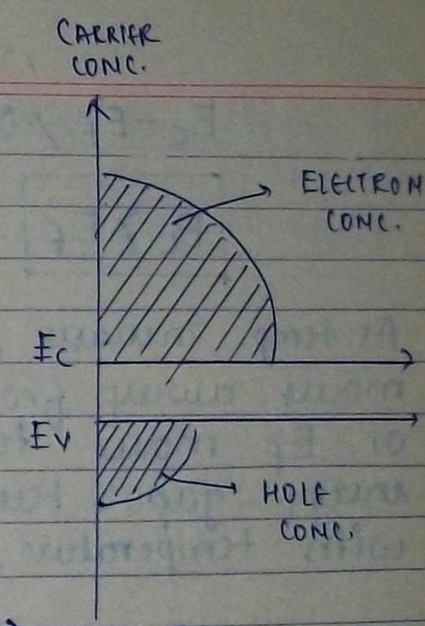
- At room temperature in n-type S.C. fermi level will be existing just below the donor energy level.

- At room temperature carrier conc. will be created and there will be conductivity in the semiconductor.

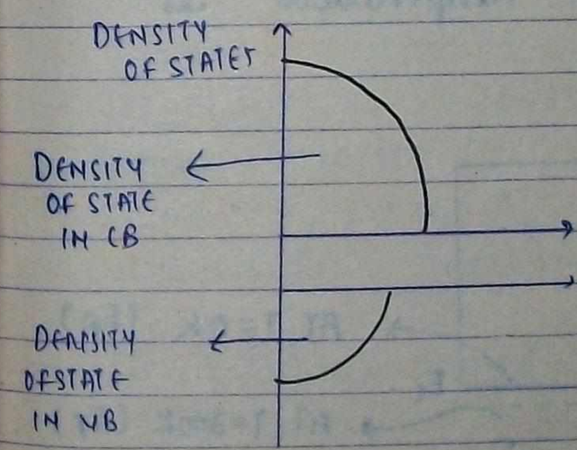
Separate diagram for:
1. Electron and hole concentration
2. fermi level diagram.
3. Density of states.



(AT T=300K)



(AT T=300K)



CASE (3): MATHEMATICAL EQUATIONS.

$$E_c - E_f = kT \log_e\left(\frac{N_c}{N_D}\right)$$

(1) LET TEMP. INCREASES -

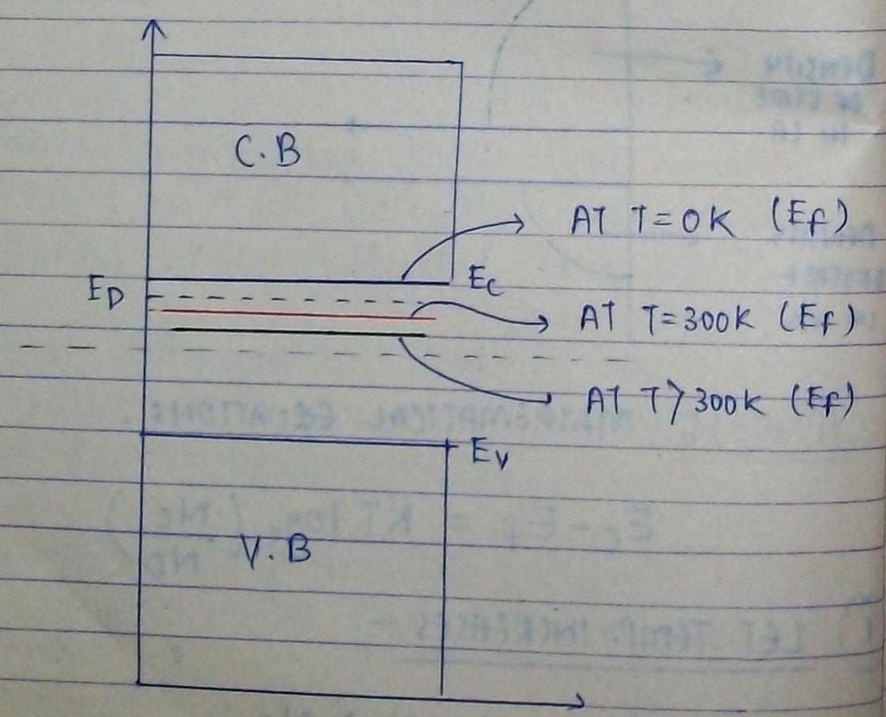
$N_c \uparrow$ and $N_c > N_D$

$E_C - E_f > 0$

$$\boxed{E_C > E_f}$$

- As temp. increases, In N-type S.C, E_f moves away from conduction band or E_f moves towards the centre of energy gap. Hence conductivity decreases with temperature.

The position of fermi level in N-type S.C. for different temperatures is given below:



- At curie temp, in the N-type S.C. the fermi-level will be existing at the middle or centre of the energy gap. (means S.C become intrinsic).

(2) LET DOPING INCREASES –

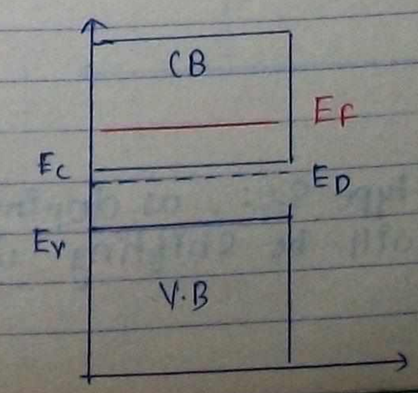
$N_D \uparrow$ and let $N_D > N_C$

$E_C - E_f < 0$

$$\boxed{E_C < E_f}$$

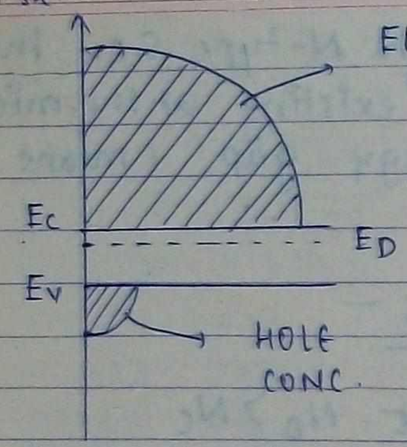
- In N type S.C as doping (N_D) increases, E_f moves into the CB (or) E_f moves away from the centre of energy gap. Hence the conductivity increases with temperature.

- In a highly doped N-type S.C. or highly degenerative N-type S.C., the fermi level will be existing in the conduction band.



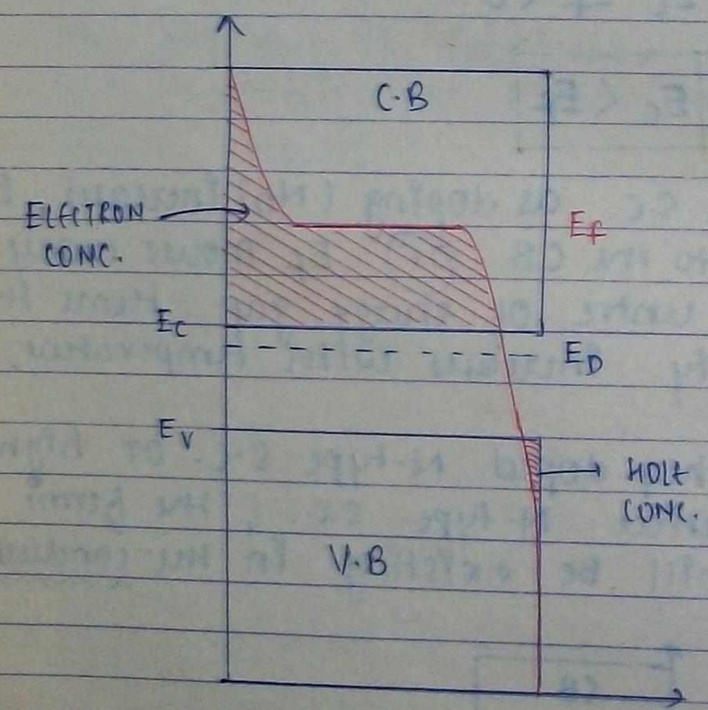
N^+ S.C.
AT T = 300K

e^- AND HOLE CON. IN N-T S.C.



ELECTRON CONC. >> HOLE CONC.

COMBINE DIAGRAM –



NOTE –

In the N-type S.C., as doping increase the fermi level will be shifting upward

CASE (4): SHIFT IN THE POSITION OF E_f DUE TO DOPING

(OR)

SHIFT IN THE POSITION OF E_f wrt E_f of INTRINSIC S.C

(OR)

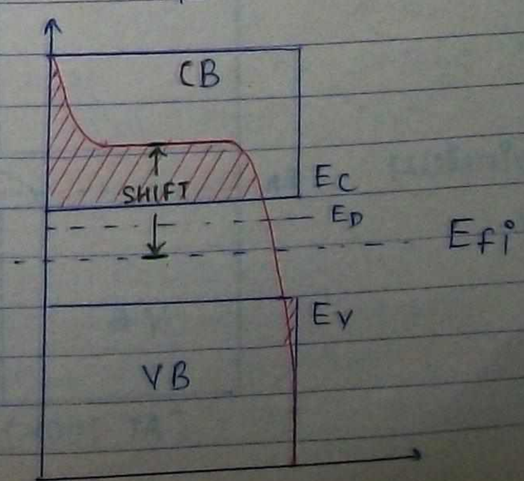
SHIFT IN THE POSITION OF E_f wrt CENTRE OF ENERGY GAP.

$$\boxed{\text{SHIFT} = KT \log_e \frac{N_D}{n_i} \; eV}$$

(or)

$$\boxed{\text{SHIFT} = KT \log_e \frac{n}{n_i} \; eV}$$

NOTE - In n-type shift is upward (+ve).



⇒ FERMI-LEVEL IN P-TYPE SEMICONDUCTOR –

$$P \simeq N_A$$

$$N_V e^{-(E_f - E_V)/kT} \simeq N_A$$

$$\frac{N_V}{N_A} = e^{(E_f - E_V)/kT}$$

$$\boxed{E_f - E_V = kT \log_e\left(\frac{N_V}{N_A}\right)}$$

$$\boxed{E_f = E_V + kT \log_e\left(\frac{N_V}{N_A}\right)}$$

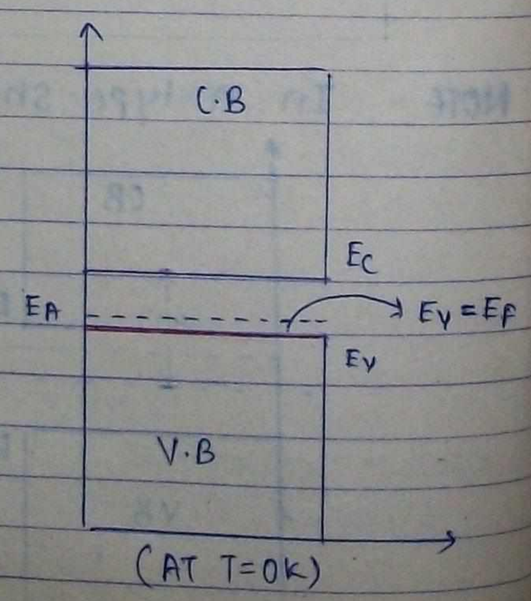
- In the p-type S.C. fermi level is a function of temp and doping concentration.

CASE (1): AT T=0K

$E_f = E_V$

↓

means E_f coincides with E_V.

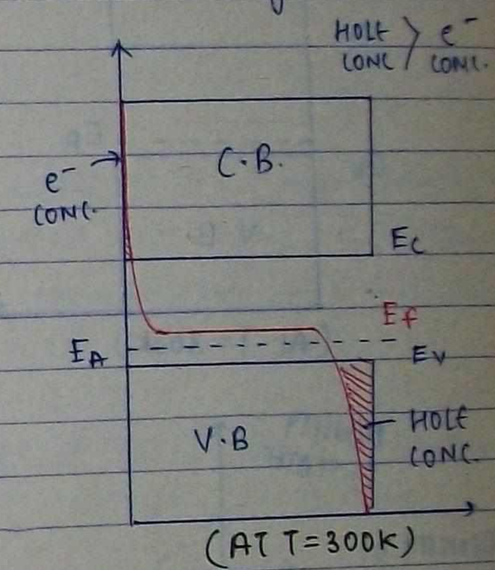


- At t=0K carrier conc. are zero and therefore conductivity is zero, hence p-type S.C at zero kelvin will be working as an insulator.

CASE (2): AT T=300K

$$\boxed{E_f = E_V + kT \log_e \frac{N_V}{N_A}}$$

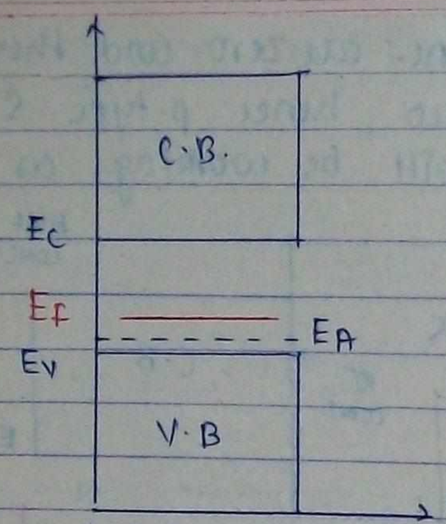
where T=300K and N_V value must be taken for 300K.



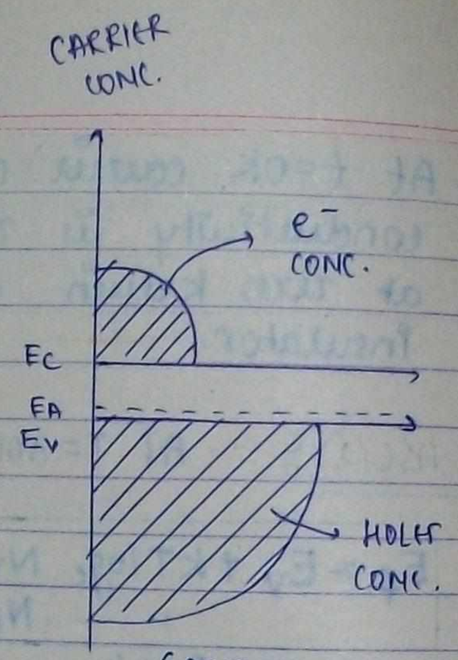
- In p type semiconductor, at room temp, the fermi level will be existing just above the acceptor energy level.

- At room temperature because of thermal energy, covalent bonds will be broken and there will be majority & minority carriers and there will be a conductivity in the S.C.

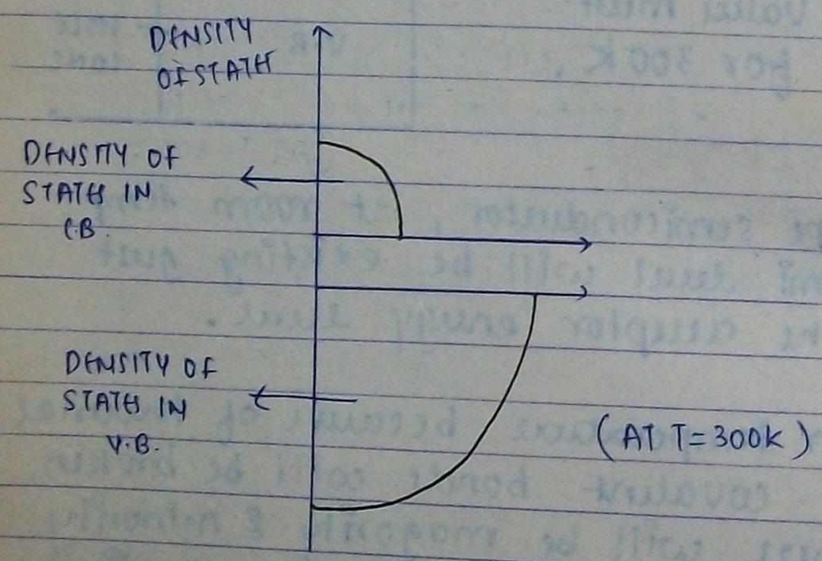
Separate diagram:
1. location of fermi level
2. carrier concentration
3. density of states



(AT T=300k)



(AT T=300k)



(AT T=300k)

CASE (3): MATHEMATICAL EQUATIONS

$$E_f - E_V = KT \log_e \frac{N_V}{N_A}$$

(1) LET TEMP. INCREASES -

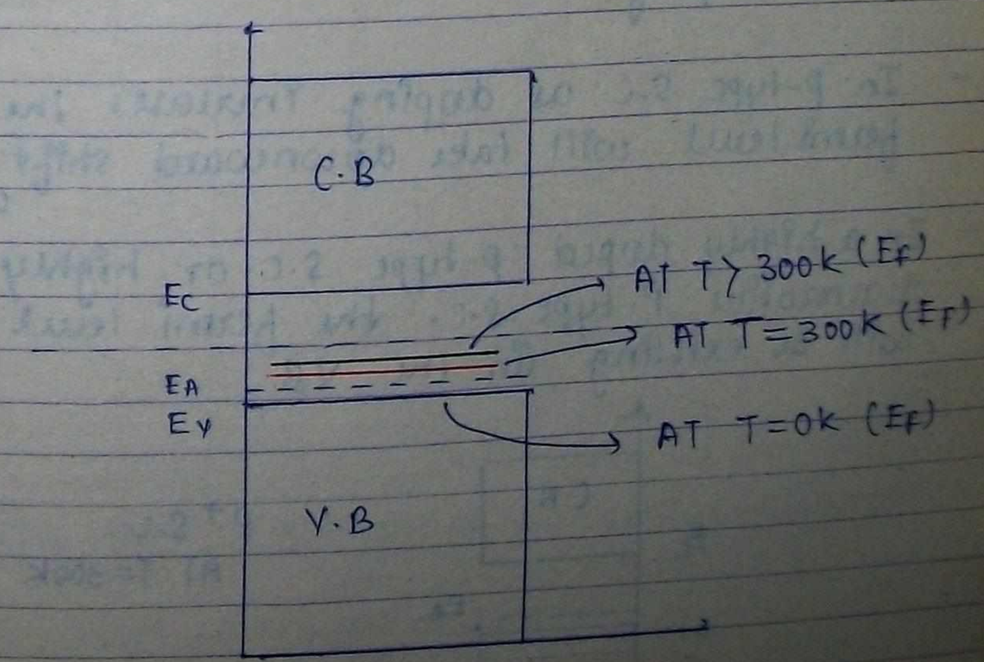
$N_V \uparrow$ and let $N_V > N_A$

$$E_f - E_V > 0$$

$$E_f > E_V$$

- In p type semiconductor as temp increases E_f moves away from VB (OR) E_f moves towards the centre of energy gap. Hence conductivity decreases with temp.

The position of fermi level in the p-type S.C. for different temp is given below:



- In p type S.C at curie temp., fermi level will be existing at the middle of the energy gap.

(2) WHEN DOPING INCREASES –

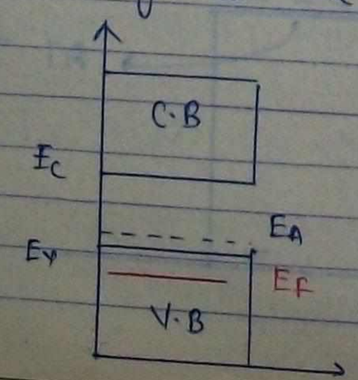
$N_A \uparrow$ and let $N_A > N_V$

$E_f - E_V < 0$, $\boxed{E_f < E_V}$

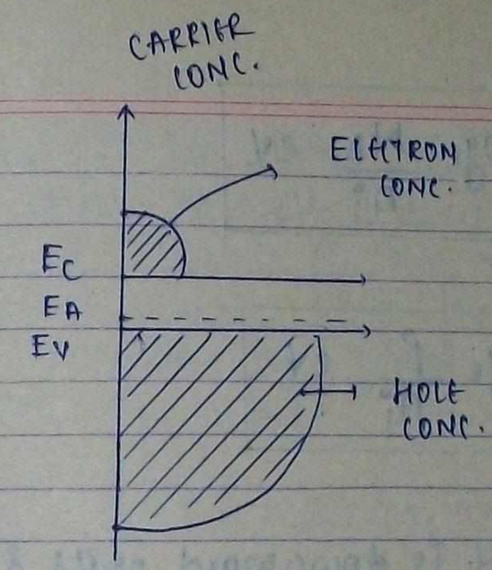
- In P-type semiconductor as doping (N_A) increase, E_f moves into the VB (or) E_f moves away from the centre of energy gap hence conductivity increases with doping.

- In P-type S.C as doping increases the fermi level will take downward shift. (-ve)

- In a highly doped p-type S.C or highly degenerative P-type S.C. the fermi level will be existing in the VB.

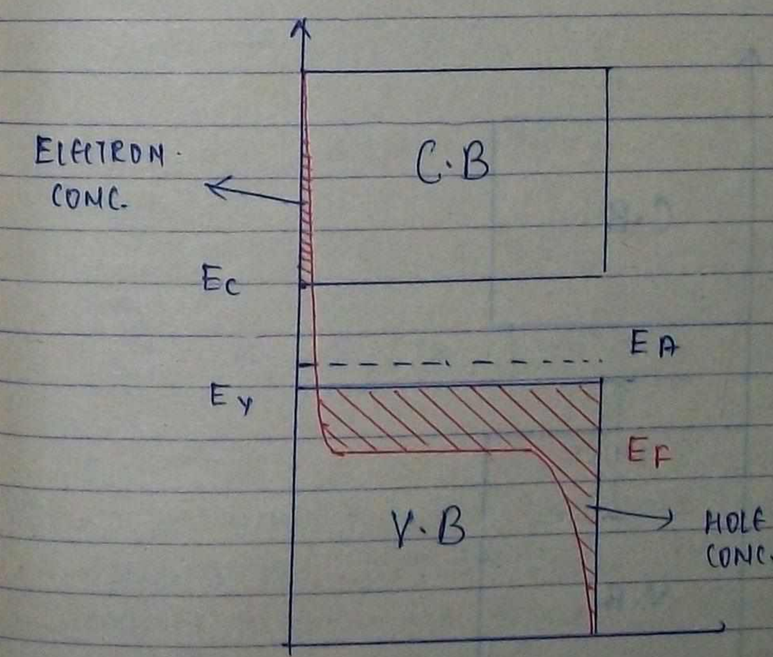


P^+ S.C. AT T=300K



P^+ S.C. AT T=300K

COMBINE DIAGRAM.



P^+ S.C AT T=300k

CASE (4) : SHIFT IN POSITION OF E_F DUE TO DOPING

(OR)

SHIF IN POSITION OF E_F WRT INTRINSIC S.C.

(OR)

SHIFT IN POSITION OF E_F WRT CENTRE OF ENERGY GAP.

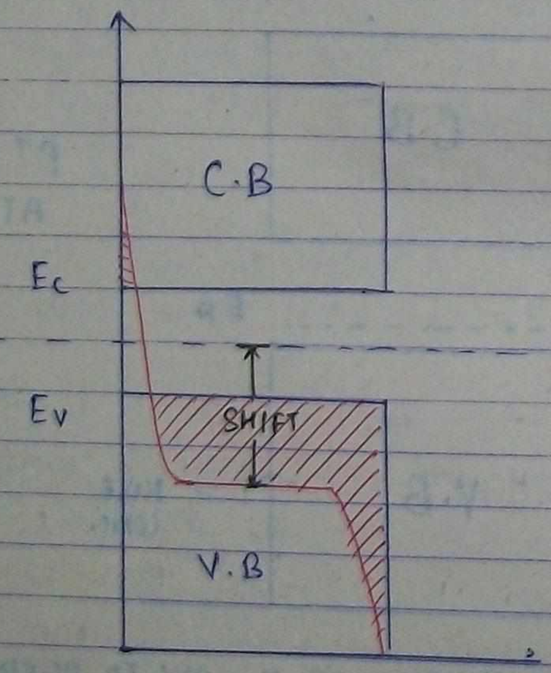
$$\text{SHIFT} = kT \log_e\left(\frac{\text{DOPING CONC.}}{n_i}\right)$$ Generalised formula.

$$\boxed{\text{SHIFT} = kT \log_e \frac{N_A}{n_i} \text{ eV}}$$

$$\boxed{\text{SHIFT} = kT \log_e \frac{P}{n_i} \text{ eV}}$$

NOTE -

In P type S.C. It is downward shift & is denoted by -ve sign.



Que. In an n-type S.C. the fermi level lies 0.3 eV below the cond^n band at 300K, If the temp is increased to 330K find the approx. new position of fermi-level.

Sol^n: for n type S.C -

$$E_C - E_f = kT \log_e \frac{N_C}{N_D}$$

neglecting the variation of N_C with temp

$$E_C - E_f \propto T$$

$$0.3 \text{ eV} \propto 300 \quad -(1)$$

$$E_C - E_{f_2} \propto 330 \quad -(2)$$

$$E_C - E_{f_2} = \frac{330 \times 0.3}{300} = 0.33 \text{ eV}$$

Que. In an n type S.C the fermi level lies 0.4 eV below the cond^n. band If the conc. of donor atoms is doubled find the new position of fermi level. assume $kT = 0.03$ eV

Sol^n: for n type.

$$N_D \simeq N_C e^{-(E_C - E_f)/kT}$$

$$N_D = N_C e^{-0.4/0.03} \quad -(1)$$

$$2N_D = N_C e^{-(E_C - E_{f_2})/0.03} \quad -(2)$$

(1)/(2)

$$\frac{1}{2} = e^{-\frac{0.4}{0.03} + \frac{(E_C - E_{f_2})}{0.03}}$$

$$\log(0.5) = -\frac{0.4}{0.03} + \frac{(E_C - E_{f_2})}{0.03}$$

$$E_C - E_{f_2} = 0.4 + 0.03 \log(0.5)$$

$$= \underline{\underline{0.379 \text{ eV}}}.$$

Qu. In a P-type S.C., the fermi level lies 0.4 eV above the VB if the conc. of acceptor atoms is trippled. find the new position of fermi level. assume $kT = 0.03$ eV.

Soln: P-type S.C -

$$N_A = N_V e^{-(E_f - E_V)/kT}$$

$$\frac{N_A}{3N_A} = \frac{N_V e^{-0.4/0.03}}{N_V e^{-(E_{f_2} - E_V)/0.03}}$$

$$E_{f_2} - E_V = \underline{\underline{0.367}} \text{ eV}.$$

Qu. In a S.C. at room temp, the intrinsic carrier conc. and resistivity are $1.5 \times 10^{16}/m^3$ and $2 \times 10^{13}\ \Omega m$ resp. If is converted into an extrinsic S.C. with a doping conc. of $10^{20}/m^3$. find the shift in the fermi level due to doping.

Soln:

$$n_i = 1.5 \times 10^{16}/m^3, \quad \rho_i = 2 \times 10^{13}\ \Omega m$$

$$\text{doping conc} = 10^{20}/m^3, \quad T = 300k$$

$$\text{SHIFT} = kT \log_e \left(\frac{\text{DOPING CON.}}{n_i} \right) \text{ eV}$$

$$= 8.62 \times 10^{-5} (300) \log_e \frac{10^{20}}{1.5 \times 10^{16}}$$

$$= \underline{\underline{0.227 \text{ eV}}}$$

Qu. Si is doped with Boron to a conc. of 4×10^{17} atoms/cm^3, assume the intrinsic carrier con. 1.5×10^{10} atom/cm^3 and $T = 27°C$, compare to undoped Si, the fermi level of doped Si is ___.

Soln: Boron → P type semicond^n.

$$\text{Shift} = kT \log \frac{N_A}{n_i} \text{ eV}$$

$$= 8.62 \times 10^{-5} \times 300 \times \log_e \frac{4 \times 10^{17}}{1.5 \times 10^{10}} \text{ eV}$$

shift = 0.44 eV.

in p type S.C it is a downward shift

(OR)

SHIFT = − 0.44 eV.

Que. P-10 Que 1. (convential question).

Soln: $\rho_i = 3000\ \Omega m$

$n_i = 1.1 \times 10^6 / m^3$

$\mu_n = 3\mu_p$

$$\rho_i = \frac{1}{n_i q(\mu_n + \mu_p)}$$

$$\rho_i = \frac{1}{n_i q(4\mu_p)} \qquad (\mu_n = 3\mu_p)$$

$$\mu_p = \frac{1}{4 n_i q \rho_i} = \frac{1}{4 \times 1.1\times10^6 \times 1.6\times10^{-19} \times 3000}$$

$\mu_p = 473 \times 10^6\ m^2/Vsec$

$\mu_n = 3\mu_p$

$\mu_n = 1420 \times 10^6\ m^2/Vsec$

Que. P-10. Que 2.

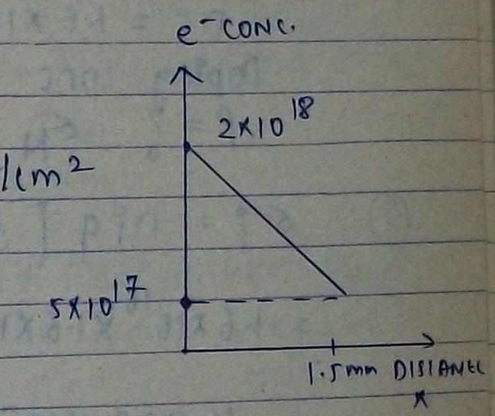
Soln: T = 300k (N type)

n varies from 2×10^{18} to $5\times10^{17}/cm^3$

distance $x = 1.5mm$

$J_n(diff) = 360\ A/cm^2$

μ_n -



$$J_n(diff) = q D_n \cdot \frac{dn}{dx}$$

$$360 = 1.6\times10^{-19} \times D_n \left[\frac{5\times10^{17} - 2\times10^{18}}{1.5\times10^{-1} - 0}\right]$$

$D_n = -225\ cm^2/sec$

NOTE - D_n cannot be negative

$D_n = 225\ cm^2/sec$

$D_n = \mu_n V_T$ $\qquad (V_T = 26mV)$ room temp

$$\mu_n = \frac{D_n}{V_T} = \frac{225}{26\times10^{-3}}$$

$\mu_n = 8653\ cm^2/Vsec.$

Que. P-10, Q 3.

Solⁿ: $\mu_n = 0.125\ m^2/Vsec$

$\mu_p = 0.048\ m^2/Vsec$

$\sigma_i = -$ $T = 300k$

$n_i = 1.6 \times 10^{16}$ atoms/m^3

Doping conc $= 10^{23}$ atom/m^3

$\rho = ?$ $\sigma_N = ?$ shift = –

① $\sigma_i = n_i q [\mu_n + \mu_p]$

$= 1.6 \times 10^{16} \times 1.6 \times 10^{-19} [0.125 + 0.048]$

$= \underline{\underline{4.428 \times 10^{-4}}}\ \mho/m.$

② $\rho = \dfrac{n_i^2}{\text{Doping con.}}$ (N type)

$= \dfrac{(1.6 \times 10^{16})^2}{10^{23}}$

$= \underline{\underline{2.56 \times 10^{9}}}\ /m^3$

③ $\sigma_n = N_D q \mu_n$

$= 10^{23} \times 1.6 \times 10^{-19} \times 0.125$

$= \underline{\underline{2000}}\ \mho/m$

④ SHIFT $= kT \log_e \dfrac{N_D}{n_i}$ eV

$= 8.62 \times 10^{-5} (300) \log_e \dfrac{10^{23}}{1.6 \times 10^{16}}$ eV

$= \underline{\underline{0.404}}$ eV

N-type semiconductor ∴ it is upward shift.

Que. P-10 Que 2 (A).

FERMI DIRAC PROBABILITY DISTRIBUTION FUNⁿ –
Refer to EDC practise book Page 26

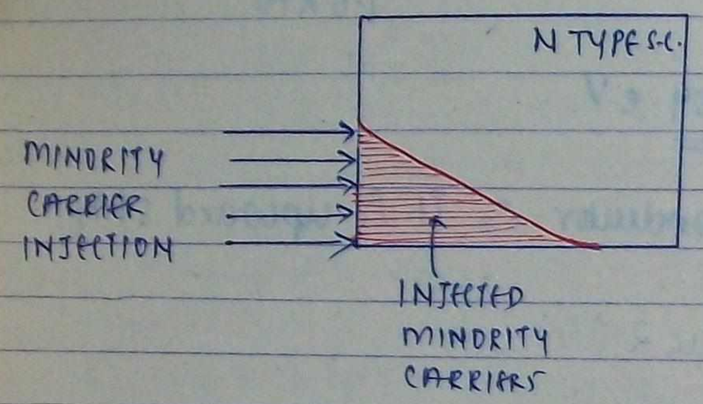
$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

also $N_p + p = N_A + n.$

Que.

21/7/11

⇒ MINORITY CARRIER INJECTION INTO THE S.C -



- when minority carriers are injected into the S.C. bar, the injected minority carriers will be maximum on the surface of the S.C. where they are introduced and the injected minority carrier conc. gradually decreases into the S.C. (depth).

- when a hole is introduced in the n-type S.C. bar the injected holes will be moving in the S.C. from higher conc. to lower conc. ie due to the property called diffusion.

⇒ WHEN AN S.C IS SUBJECTED TO DONAR & ACCEPTOR IMPURITIES -

(1) If $N_A = N_D$ is applied :
S.C. remain intrinsic

(2) If $N_A > N_D$ is applied :
S.C. Turns P-type.

(3) If $N_A < N_D$ is applied :
S.C. Turns N-type.

- In a ptype S.C. having auptor conc. N_A of 2×10^{16} atom/cm³ is subjected to donar impurities to the extent of 2.5×10^{16} atoms/cm³ the semiconductor is N-TYPE and majority carrier a ELECTRON with a conc. of 0.5×10^{16} atom/cm³

Que. A 25 gm of P-type Ge crystal exhibit a resistivity of 5 Ωcm at 300 K, by uniform antimony doping, it is converted into n-type S.C. having 1 Ωcm resistivity at 300 K, If each atom of the initial auptor impurity is exactly neutralised by one atom of antimony. find in microgms the ator amount of antimony required.

Density of Ge = 5.32 gm/cm³,
No. of Sb atom/gm = 5×10^{21}, $\mu_n = 3800$ cm²/Vs
$\mu_p = 1800$ cm²/Vsec, $q = 1.6 \times 10^{-19}$ C.

Soln: Before antimony is applied, the S.C is p-type with a resistivity $\rho_p = 5$ Ωcm and therefore its auptor

conc. or hole conc. is given by:

$$\rho_p = \frac{1}{N_A \cdot q \cdot \mu_p}$$

$$N_A = \frac{1}{\rho_p \cdot q \cdot \mu_p}$$

$$p \simeq N_A = \frac{1}{5 \times 1.6 \times 10^{-19} \times 1800} = 6.94 \times 10^{14} / cm^3$$

$$p \simeq N_A \simeq 6.94 \times 10^{14} / cm^3$$

By adding (Sb) atoms, the p type S.C. is converted into n-type S.C. with a resistivity of 1 Ωcm and donor conc. or electron conc. in the S.C is:

$$N_D = \frac{1}{\rho_N \cdot q \cdot \mu_n}$$

$$= \frac{1}{1 \times 1.6 \times 10^{-19} \times 3800}$$

$$n \simeq N_D \simeq 16.45 \times 10^{14} / cm^3$$

This is the net e- conc. after neutralizing the initial holes of the p type S.C.

The no. of (Sb) atom required per cm^3 is

$$= 6.944 \times 10^{14} + 16.45 \times 10^{14}$$

$$= 23.394 \times 10^{14} \text{ atom}/cm^3$$

$$\text{VOLUME} = \frac{\text{WEIGHT}}{\text{DENSITY}}$$

25 gms of Ge has:

$$\text{Volume} = \frac{25 \text{ gm}}{5.32 \text{ gm}/cm^3} = 4.699 \text{ cm}^3$$

Total no. of antimony atoms required:

$$= 23.394 \times 10^{14} \text{ atom}/cm^3 \times 4.699 \text{ cm}^3$$

$$= 109.928 \times 10^{14} \text{ atom.}$$

5×10^{21} Sb atoms = 1 gm

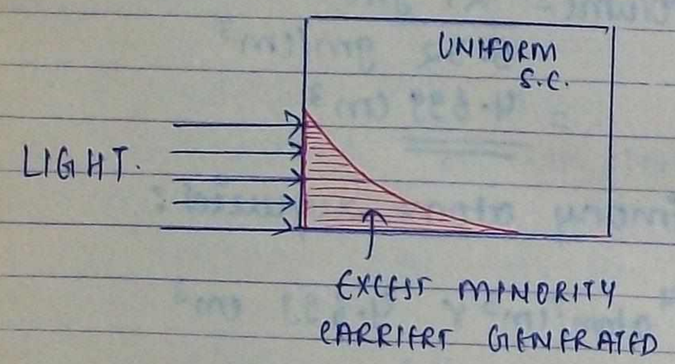
$$109.928 \times 10^{14} \text{ Sb atoms} = \frac{109.928 \times 10^{14}}{5 \times 10^{21}} = 2.1985 \ \mu\text{gms}$$

⇒ LOW LEVEL INJECTION –

- It means the conc. of magority carriers is far greater than the conc. of minority carriers.

- under low level injection, light is focused on the semiconductor and then we analyse photoelectric properties.

⇒ LIGHT FALLING ON A S.C. –



- when light is focused on a S.C. bar, because of photon energy the surface of the S.C. gets heated up and due to the thermal energy a number of covalent bonds will be broken creating electrons and holes.

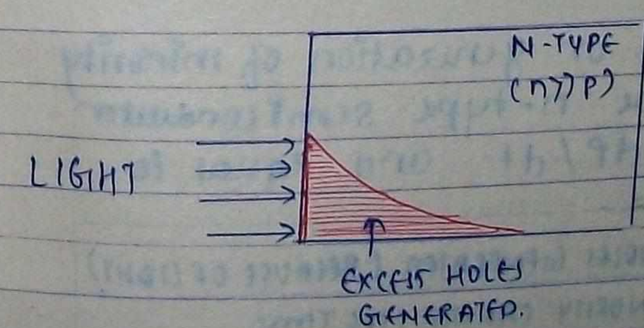
- under steady state condition:
  $\Delta n = \Delta p$.

- The minority carrier conc. will be increasing and the magority carrier conc. will remain almost a constant.

- The ingected minority carrier conc. will be maximum on the surface where light is focused and it is gradually reduced into the depth of the S.C.

- The ingected minority carrier conc. in the S.C. will be moving from higher conc. to lower conc. ie due to the property called diffusion.

- when light falls on the n-type S.C. holes are generated in the S.C and this holes will be moving in the S.C., from higher conc. to lower conc. ie. due to the property called diffusion.



- when light falls on the S.C. minority carriers will be generated.

- when light falls on the N type S.C under low level injection, there will be two current components :
  1. hole drift current
  2. hole diffusion current.

- under low level injection, hole drift current in the N type S.C is almost negligible.

- In n-type S.C. under low level injection current is dominated by diffusion.

- when light falls on the S.C, due to the breaking of covalent bond equal e^- and holes are generated.

- under steady state condition
  $\Delta n = \Delta p$.

- Generation rate or generation of minority carriers in the n-type semiconductor is given by dP/dt and equal to

$$\boxed{\frac{dP}{dt} = \frac{\text{EXCESS HOLES GENERATED (BECAUSE OF LIGHT)}}{\text{MINORITY CARRIER LIFE TIME}}}$$

$$\boxed{\frac{dP}{dt} = \frac{\Delta P}{\tau_p}}$$

unit of $\frac{dP}{dt}$ = e^- hole pair / cm^3 / sec.

Que. Generation rate due to irradiation in S.C., n type, $N_D = 10^{17}/cm^3$, when excess e^- conc. in the steady state is $\Delta n = 10^{15}/cm^3$ and $\tau_p = 10\,\mu sec$.

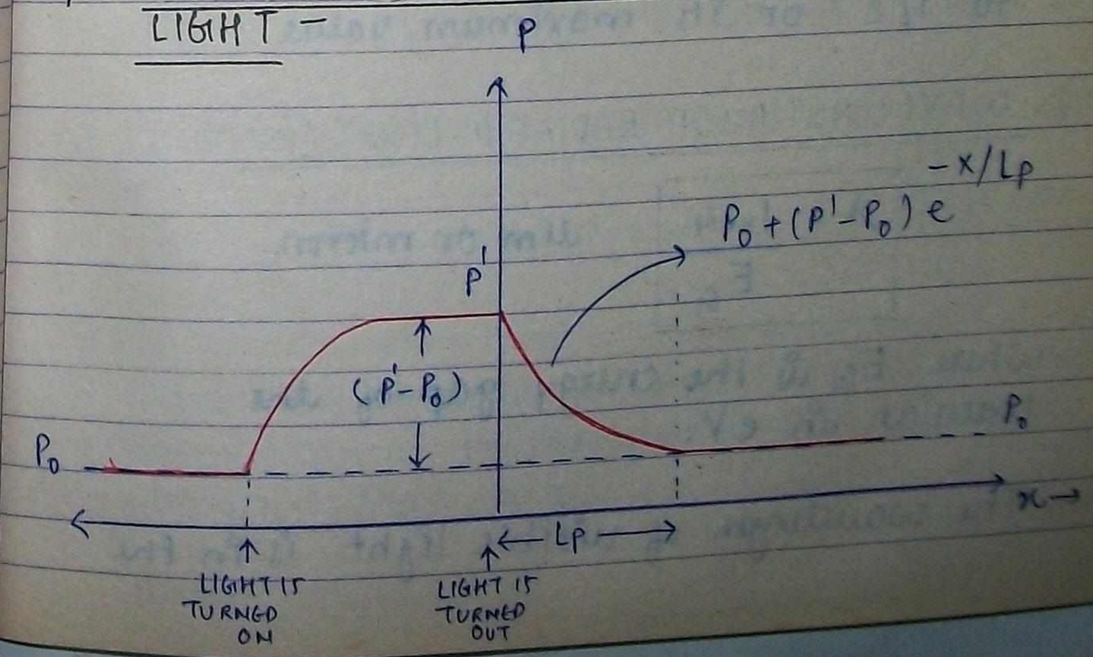
Soln:

$$\Delta p = \Delta n = 10^{15}/cm^3$$

$$\frac{dP}{dt} = \frac{\Delta P}{\tau_p} = \frac{10^{15}}{10 \times 10^{-6}}$$

$$= 10^{20} \; e^- \text{ hole pair} / cm^3 / sec.$$

⇒ CONSIDERING AN N-TYPE S.C. SUBJECTED TO LIGHT –



If $x = L_p$, If x is slightly $> L_p$

$= P_0 + (P' - P_0) e^{-1}$ $\simeq P_0 + 0$

$= P_0 + \frac{(P' - P_0)}{e}$ $\simeq P_0$

- P_0 is thermal equilibrium hole in the n type semiconductor.

- $(P' - P_0)$ is excess hole generated in the n type S.C. because of light. (it is equal to Δp).

- The length of diffusion (L_p) is define as the distance into the S.C. at which the injected carrier conc. reduces to $1/e$ or its maximum value.

⇒ WAVELENGTH OF RADIATED LIGHT (λ) –

$$\lambda = \frac{1.24}{E_G} \quad \mu m \text{ or micron.}$$

where E_G is the energy gap of the material in eV.

- The wavelength of visible light is in the range of $\lambda = 0.38\ \mu m$ to $0.76\ \mu m$.

- If wavelength $\lambda > 0.76\ \mu m$ it belongs to infrared region.

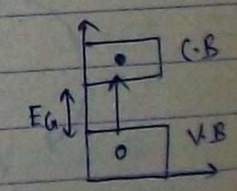
⇒ PHOTO CONDUCTIVE EFFECT –

- It is the power where conductivity of a material or device increases with the light is called photoconductive effect.

- Photoconductive effect is also called photoresistive effect.

- The property where resistivity of a material or device decreases with the light is called photoresistive effect.

⇒ PHOTO CONDUCTIVITY EQUATION –

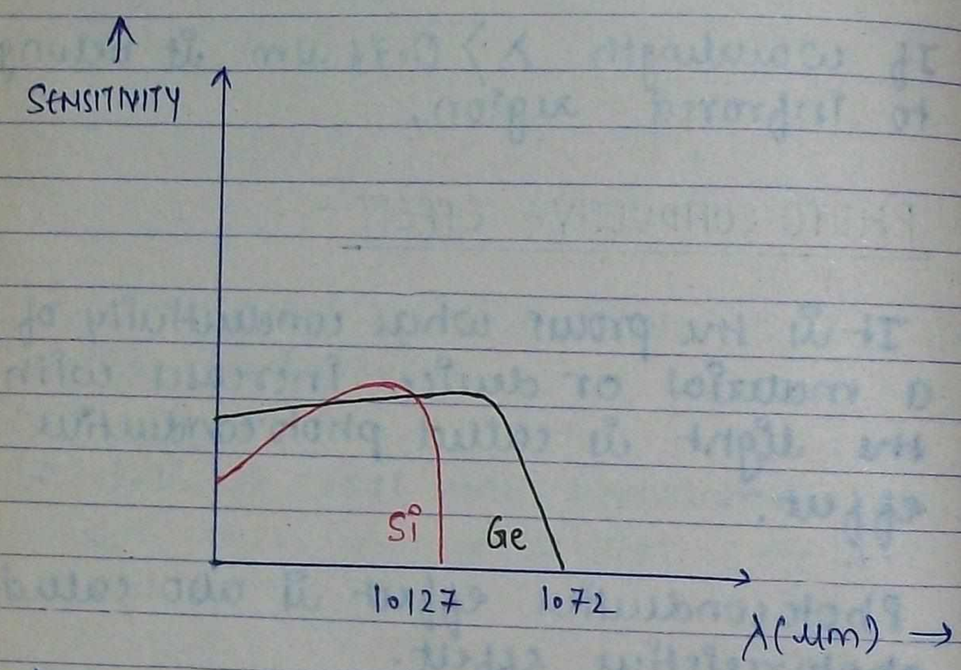


$$E_G = h\nu = \frac{hc}{\lambda}$$

- In a S.C., for an electron to excite from valence band to conduction band the photon energy required is given by:

PHOTON ENERGY $\geq E_G$ (OR) $h\nu \geq E_G$

⇒ LIGHT SENSITIVITY CURVE FOR Ge & Si –



- when compare to Si, Ge is more sensitive to photon energy.

for Ge :

$$\lambda = \frac{1.24}{0.72} = \underline{\underline{1.72\ \mu m}}$$

λ_c = cuttoff wavelength

λ_c is the cuttoff wavelength, it is the max wavelength the material will respond to light.

Similarly,

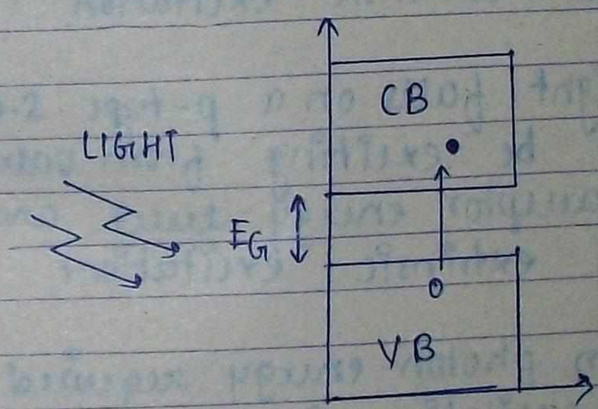
for Si :

$$\lambda = \frac{1.24}{1.1} = 1.127\ \mu m$$

$$\lambda_c = \lambda = \underline{\underline{1.127\ \mu m}}$$

⇒ INTRINSIC EXCITATION –

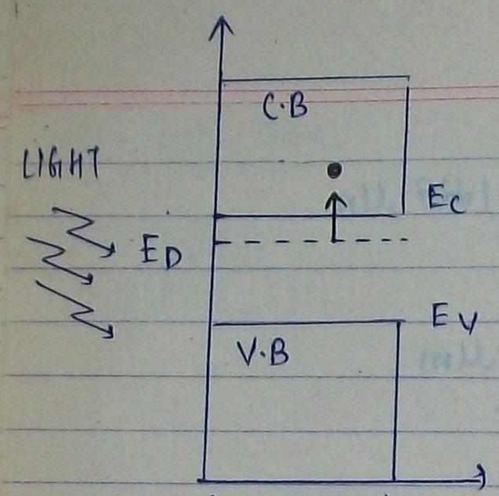
- when light falls on the S.C. an electron may be exciting from valence band to conduction band and it is called intrinsic excitation.



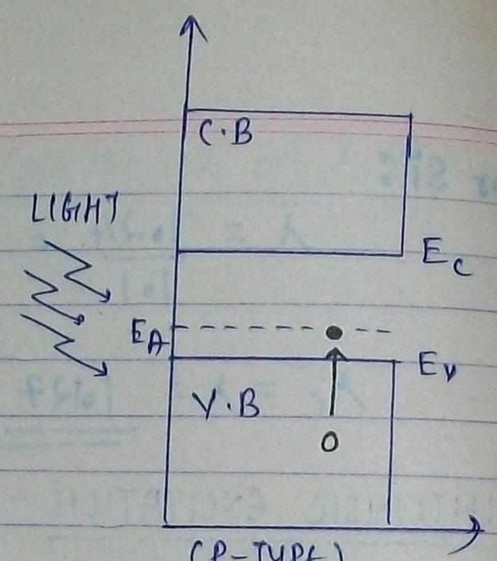
- The minimum photon energy required for intrinsic excitation is equal to its energy gap (E_G).

⇒ EXTRINSIC EXCITATION –

figure showing extrinsic excitation.



(N-TYPE)



(P-TYPE)

- when light falls on the n-type S.C, an e^- may be exciting from donar energy level into the conduction band and it is called extrinsic excitation.

- when light falls on a p-type S.C, an e^- may be exciting from valence band into acceptor energy level and it is called extrinsic excitation.

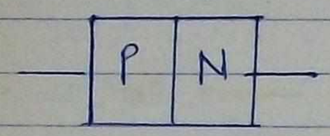
- The minimum photon energy required for extrinsic excitation is equal to
  0.01 ev for Ge
  0.05 ev for Si.

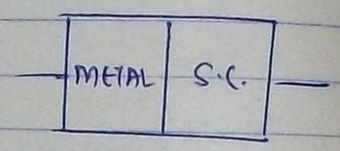
22/7/11

SEMICONDUCTOR DIODE

JUNCTION

- PN JUNCTION DIODE
- METAL S.C. DIODE





THEY CAN WORKS AS RECTIFIER

(OR)

RECTIFIER PROPERTY ARE GIVEN

DOES NOT HAVE RECTIFIER PROPERTIES

(OR)

IT CANNOT WORK AS A RECTIFIER

Ex - (1) SCHOTTKY DIODE or SCHOTTKY BARRIER DIODE

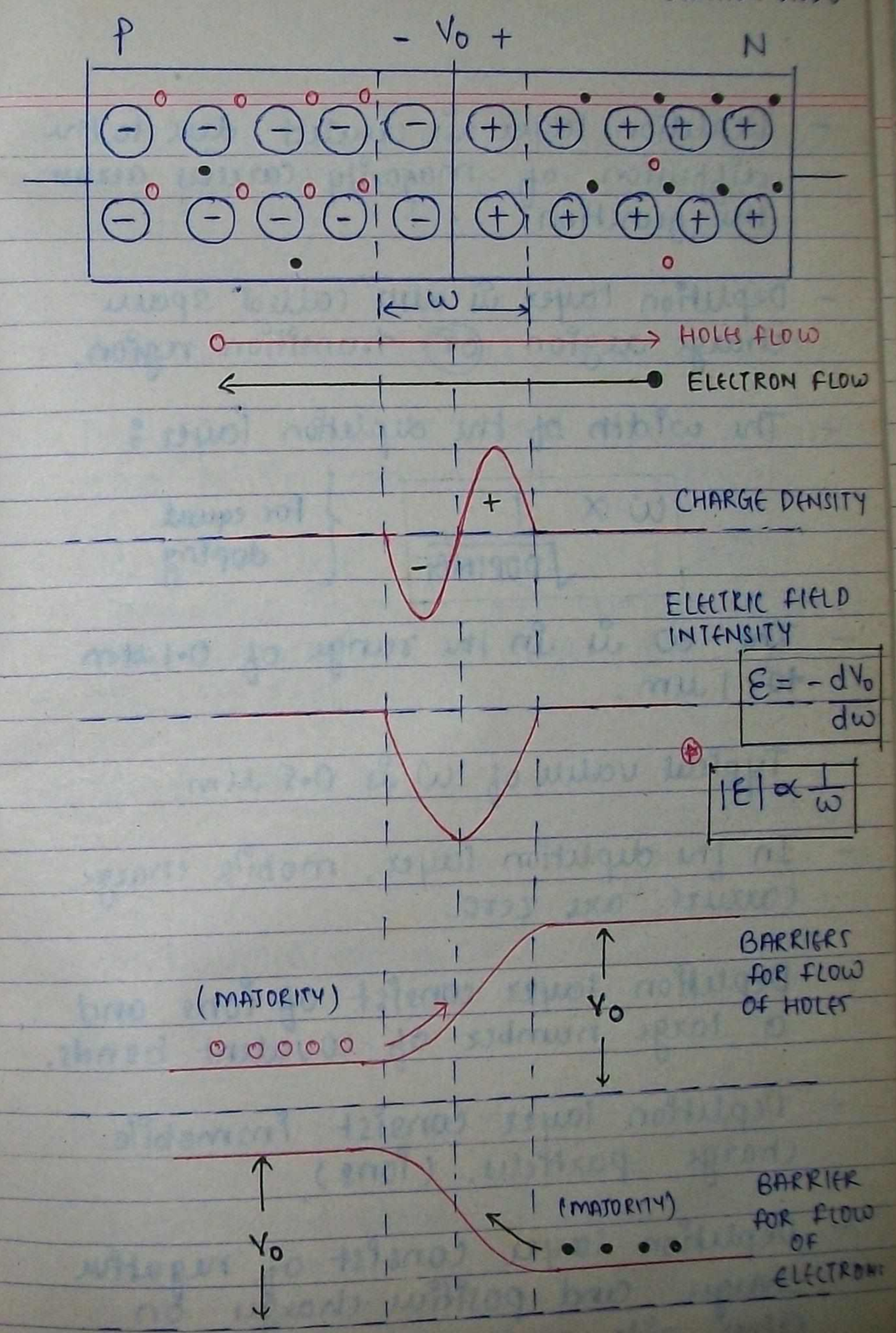
(2) POINT CONTACT DIODE

⇒ PN-JUNCTION DIODE -

- The PN junction will be formed only when a bonding force is created in between the P-type and N-type S.C.

- PN diodes are fabricated by using any one of the following methods:
  1. alloys junction technique.
  2. Grown junction technique.
  3. Diffusion junction technique.
  4. epitaxial technique.

OPEN CIRCUT PN JUNCTION DIODE



- Depletion layer is created due to the diffusion of majority carriers across the junction.

- Depletion layer is also called space charge region (or) transition region.

- The width of the depletion layer:

$$\boxed{W \propto \frac{1}{\sqrt{DOPING}}}$$ for equal doping

- The W is in the range of 0.1 μm to 1 μm.

- Typical value of W is 0.5 μm.

- In the depletion layer, mobile charge carriers are zero.

- Depletion layer consist of ions and a large number of covalent bonds.

- Depletion layer consist immobile charge particles. (ions)

- Depletion layer consist of negative charges and positive charges on either side of the junction.

- Depletion layer consist of negative ions (acceptor ions) on the P-side and positive ions (donor ions) on the N-side.

- Depletion layer opposes majority carriers.

- Depletion layer will not oppose minority carriers in crossing the junction.

- V_0 is called potential hill (or) potential barrier (or) contact potential (or) diffusion voltage (or) built in voltage (V_{bi}).

- for Ge diode:

$V_0 = 0.1\,V$ to $0.5\,V$

and typical value = 0.2 V

for Si diode:

$V_0 = 0.6\,V$ to $0.9\,V$

and typical value = 0.7 V

- In a S.C. diode contact potential is negative towards P-region and positive towards N-region.

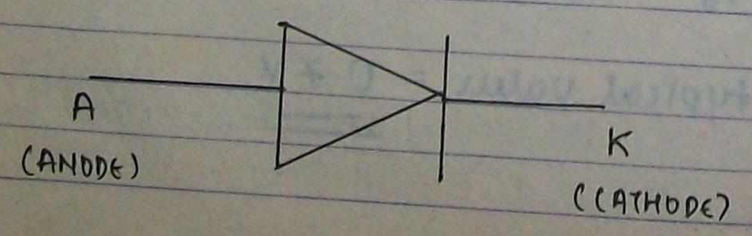
- In any type of PN-junction diode, electric field intensity ($\mathcal{E}$) is max. at the junction.

- In a normal diode field intensity is negative, and is maximum at the junction, and it tappers on either side of the junction, and it is zero outside the depletion layer.

- majority carrier will be climbing up the barrier voltage (V_0). Hence there will be an opposition.

- minority carrier will be falling down the barrier potential (V_0). Hence there will be no opposition.

⇒ DIODE SYMBOL –



- The arrow mark on the diode symbol denots the direction of forward current.

⇒ EQUATION FOR WIDTH OF DEPLETION LAYER IN OPEN CIRCUT PN-JUNCTION DIODE –

- In open circuit PN junction diode:

$$\boxed{W = \sqrt{\frac{2\mathcal{E}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) V_{bi}}} \quad \text{meters}$$

$\mathcal{E}$ = permittivity = $\mathcal{E}_0 \mathcal{E}_r$ (F/m)

* $\mathcal{E}_0$ = absolute permittivity of free space
= 8.854×10^{-12} f/m

* free space is the medium in which there are no charged particles, no ionised particles, no solid particles, no electric fields and no magnetic fields and no gravitational force is acting.

* $\mathcal{E}_r$ = relative permittivity of medium.
= 11.7 for Si
= 16 for Ge

- In open circuted diode, the width of the depletion layer depends on:

1. doping conc.
2. contact potential
3. Relative permittivity of medium.

let $N_A = N_D$ ie equal doped PN-junction

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{2}{N_A \text{ or } N_D}\right) V_0}$$

$$W \propto \frac{1}{\sqrt{N_A \text{ or } N_D}}$$

$$\boxed{W \propto \frac{1}{\sqrt{\text{DOPING}}}}$$

⇒ EQUATION FOR CONTACT POTENTIAL OF THE DIODE IN OPEN CIRCUTED PN-JUNCTION -

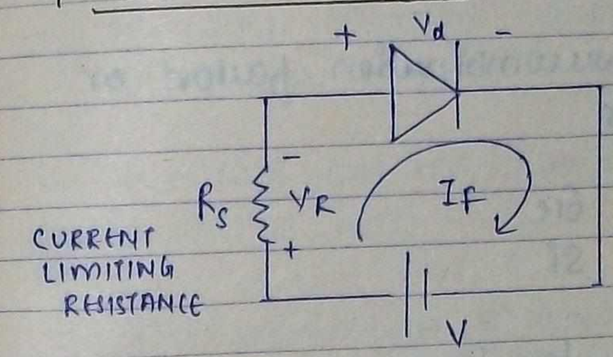
- when PN junction is open circuted :

$$\boxed{V_0 = V_T \log_e\left(\frac{N_A N_D}{n_i^2}\right)} \text{ Volts.}$$

- Contact potential of the diode depends on doping conc. and temperature.

- In a PN junction diode if doping levels are increased, then the contact potential of the diode slightly increases.

⇒ FORWARD BIASED -



$$\boxed{W \propto \frac{1}{\sqrt{\text{FORWARD BIASED.}}}}$$

$$V = V_R + V_d$$

$$V = I_f R_s + I_f R_f$$

- when PN-junction is forward biased the width of the depletion layer decreases and also the effect of barrier is nullified.

- The forward current is always only due to magority carrier

- forward current :

$$\boxed{\begin{aligned} I_f &= I_0 \left[e^{V_d/nV_T} - 1 \right] \\ I_f &\simeq I_0 \, e^{V_d/nV_T} \quad \text{Amp.} \end{aligned}}$$

where, $\eta = 1$ Ge
$= 2$ Si

- where V_T is thermal voltage (26 mV for room temp)

- η is called recombination factor or utility factor

$\eta = 1$ Ge
$= 2$ Si

also, $\eta = 1$ for large currents.
$= 2$ for smaller currents.

NOTE -

If Ge or Si is not specified, take $\eta = 1$ (default).

- V_d is forward voltage across the diode and it is always less than 1V. (below 0.5 V for Ge or below 0.9 V for Si diode).

- I_0 is reverse saturation current or minority carrier current. or leakage current.

- The forward current is only due to magority carriers, but it is mathematically derived in terms of minority carrier current.

- forward current exponentially increases with the forward voltage across diode.

- forward current flows from P to N & it is in mA.

- The minimum forward voltage required so that a current will pass through the diode is called cutin voltage (V_γ)

- Cutin voltage is also called as
  - OFFSET VOLTAGE (FET)
  - THRESHOLD VOLTAGE (BJT) & (VACCUM TUBE)
  - KNEE VOLTAGE
  - BREAK VOLTAGE

- If applied forward fo voltage is less than or equal to V_γ, forward current is zero (the diode is F.B. but non conducting)

- If the applied forward voltage is greater than V_γ then forward current will flow

and it exponentially increases with V_d.

- for Ge diode:

$V_\gamma = 0.1\,V$ to $0.5\,V$

typical value $= 0.2\,V$

for Si diode:

$V_\gamma = 0.6\,V$ to $0.9\,V$

typical value $= 0.7\,V$

- Cutin voltage decreases with temperature.

- for $1^\circ C$, $V_\gamma \downarrow$ by $2.3\,mV$

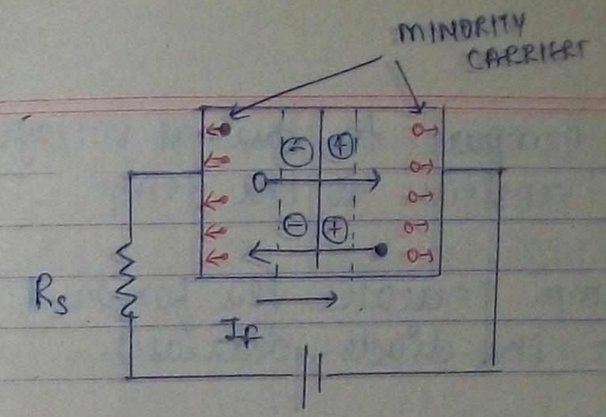
⇒ FORWARD CURRENT Vs TEMPERATURE OR EFFECT OF TEMP. ON FORWARD CURRENT –

- forward current is due to magority carrier and magority carrier conc. is almost independent of temp. Hence forward current of the diode is almost independent of temperature.

$$I_f \simeq I_0 e^{V_d/\eta V_T \uparrow}$$

$\uparrow \downarrow$ (almost independent of temp.)

NOTE –



- forward current is a diffusion current.

- In a forward biased diode, minority carriers will be moving away from the junction and therefore they will not participate in the flow of current.

- forward current is only due to magority carrier and magority carriers will be crossing the junction from higher conc. to lower conc., Hence the forward current is a diffusion current.

⇒ FORWARD VOLTAGE (V_d) Vs TEMPERATURE –

$$I_f \simeq I_0 e^{V_d/\eta T}$$

$$\boxed{V_d = \eta V_T \log_e\left(\frac{I_f}{I_0}\right)}$$

$V_d \propto V_T$

$\Delta T = 300k$ (negligible increase)

$V_T = 26\,mV$

$V_d \propto \log_e\left(\frac{\uparrow}{I_0}\right) \uparrow$

$\downarrow \quad \downarrow$

23/7/11

- when compare to thermal voltage I_0 is more sensitive to the temp.

- As temp. increases the forward voltage across the diode decreases.

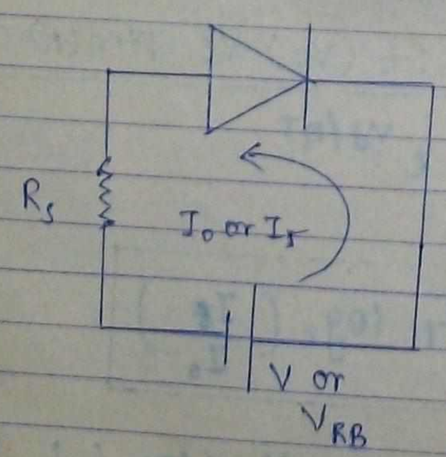
- for $1^\circ C$, V_d is ↓ by 2mV (latest)

  = by 2.5mV (old)

$$\frac{\partial V_d}{\partial T} = -2mV/^\circ C$$

⇒ REVERSE BIASED -

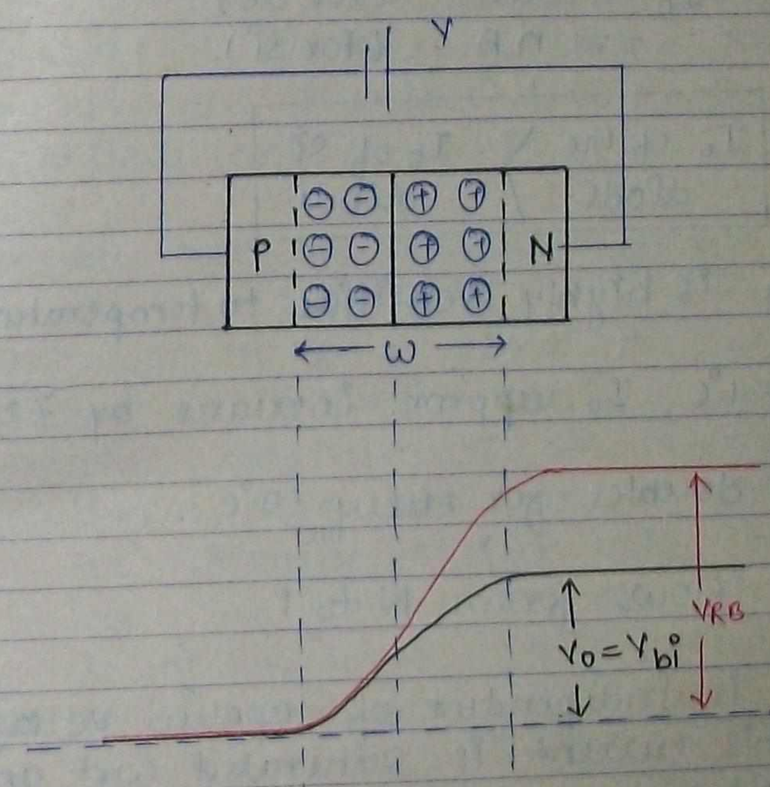
(BLOCKING BIAS)
OR
(BACK - BIAS)



$\omega \propto \sqrt{\text{REVERSED BIAS VOLTAGE}}$

- when an PN-junction is reversed biased

1. The width of the depletion layer increased
2. The barrier height will be increased.



WIDTH OF DEPLETION LAYER , Junction voltage = Sum of V_0 & V_{RB}

$\omega \propto \sqrt{V_j}$

$\omega \propto \sqrt{V_{bi} + V_{RB}}$

$\boxed{\omega \propto \sqrt{V_{RB}}}$

$V_j = V_{bi} + V_{RB}$

$(V_{bi} << V_{RB})$

$V_j \simeq V_{RB}$ $\boxed{V_j \simeq V_{RB}}$

- The reverse current I_0 is called minority carrier current or reverse saturation current or leakage current or thermally generated current.

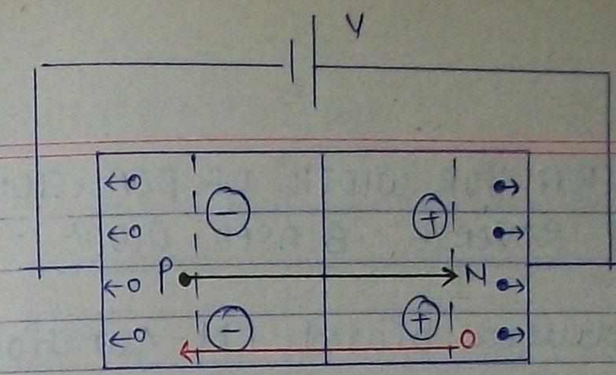
$I_0 = \mu A$ (for Ge)
$= nA$ (for Si)

$$\boxed{I_0 \text{ of Ge diode} > I_0 \text{ of Si diode.}}$$

- I_0 is highly sensitive to temperature.
- for 1°c, I_0 approx. increases by 7%.
- I_0 doubles for every 10°c.
- I_0 flows from N to P.
- I_0 is independent of applied voltage. (this current is saturated wrt applied voltage)

$$\boxed{I_{0(T_2)} = I_{0(T_1)} \left[2^{(T_2 - T_1)/10} \right]} \text{ Amp.}$$

where $T_2 > T_1$



- In a reversed biased diode, the majority carrier will be moving away from the junction and therefore they will not contribute any current.
- Reverse current is drift current.
- In a reverse bias diode the current is due to minority carriers and the minority carriers will be crossing the junction from low conc. to high conc. or the minority carriers will be crossing the junction under the influence of electric field intensity. Hence reverse current is drift current.
- The majority carriers are blocked in crossing the junction and therefore the reverse bias is called BLOCKING BIAS.

⇒ EQUATION FOR WIDTH OF DEPLETION LAYER IN A REVERSE BIASED DIODE -

- In reverse biased PN-junction:

$$\boxed{w = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0+V_{RB})}} \text{ metre}$$

or

$$\boxed{w = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)V_j}}$$

$$\boxed{w \propto \sqrt{V_j}} \quad \text{or} \quad \boxed{w \propto \sqrt{V_{bi}+V_{RB}}}$$

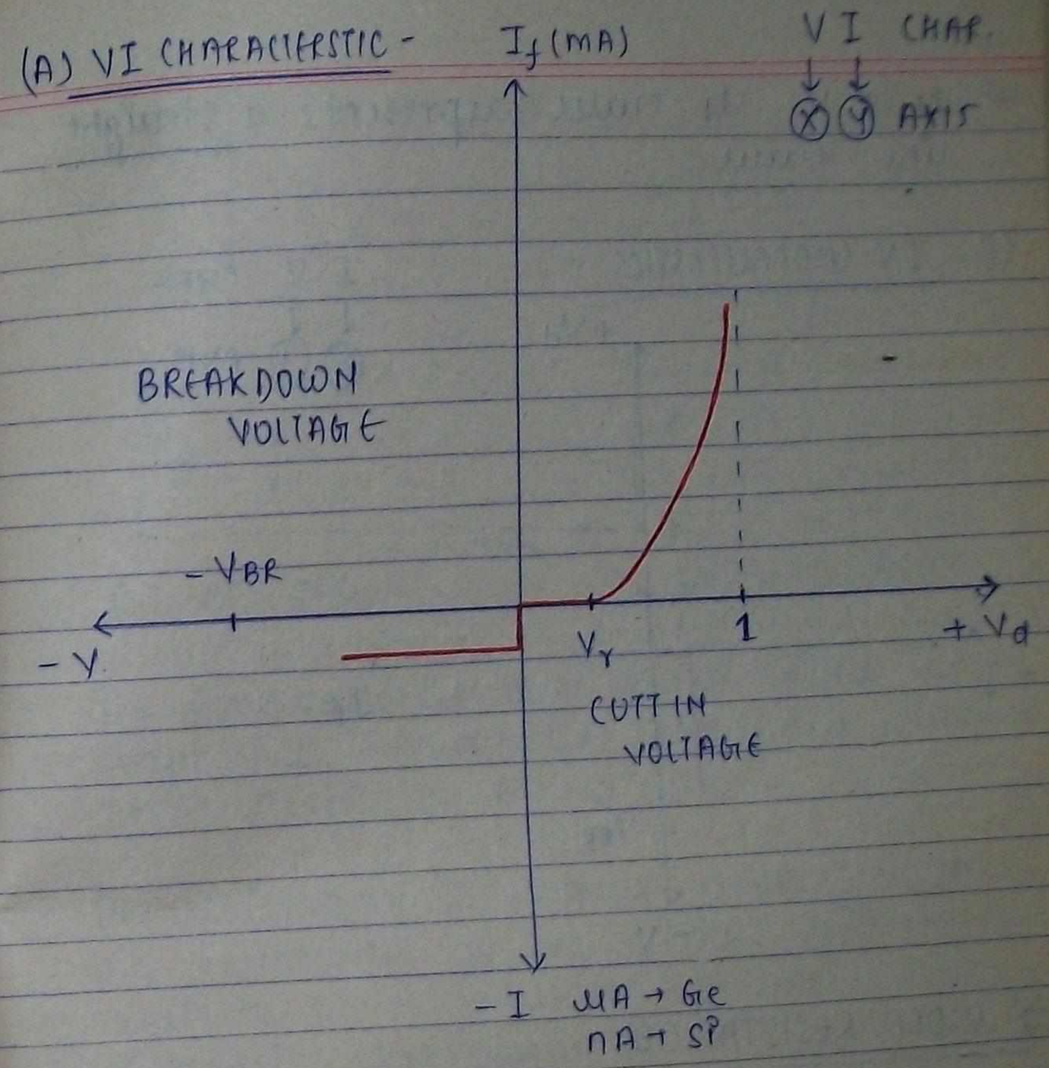
⇒ VI - CHARACTERSTICS OF DIODE -

(VOLT-AMP. CHARACTERSTIC)

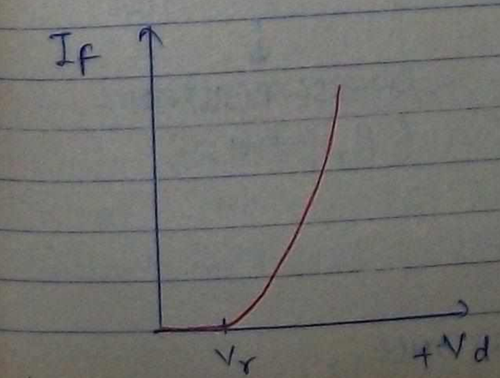
- Diode is a non linear device, active component and also unidirectional device.

- When diode is reversed biased the reverse voltage must be always less than breakdown voltage of the device. (otherwise the diode will be destroyed)

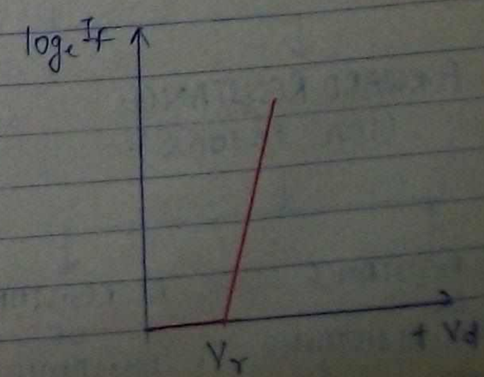
(A) VI CHARACTERSTIC -



(B) I_f Vs V_d CURVE -



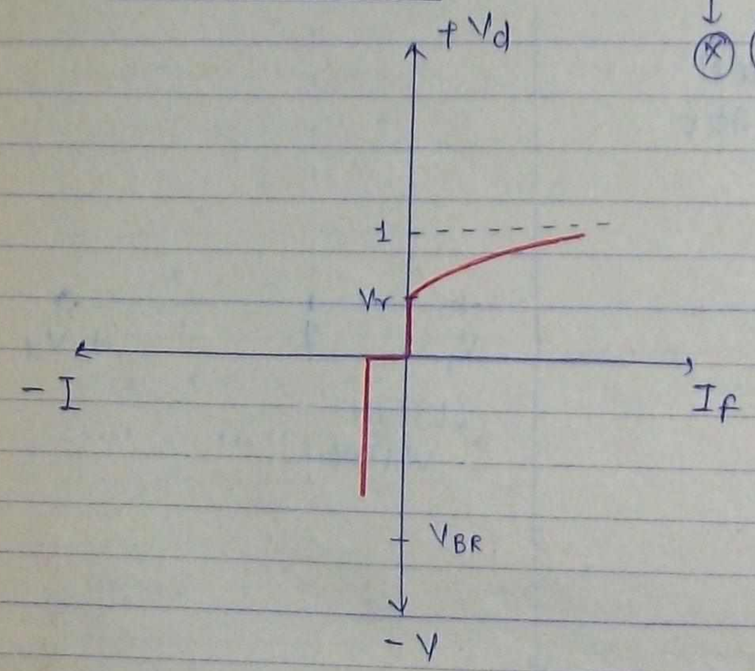
(C) Log I_f Vs V_d CURVE -



- log I_f vs V_d curve represents a straight line curve.

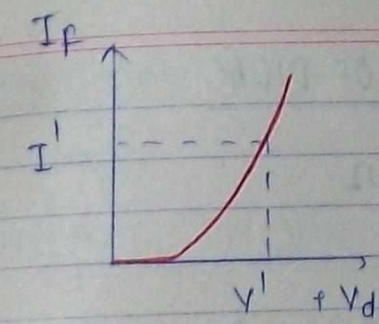
(D) IV CHARACTERSTICS -

I V CHAR.
↓ ↓
(X) (Y) AXIS.



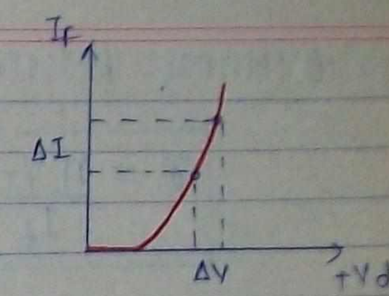
⇒ DIODE RESISTANCE -

DIODE RESISTANCE
- FORWARD RESISTANCE (10Ω to 100Ω)
  - DC RESISTANCE OR STATIC RESISTANCE (R_f)
  - AC RESISTANCE OR DYNAMIC RESISTANCE (r)
- REVERSE RESISTANCE ($R_r > 1M\Omega$)



$$R_f = \frac{V'}{I'}$$

D.C. RESISTANCE



$$r = \frac{\partial V}{\partial I} = \frac{\Delta V}{\Delta I}$$

AC RESISTANCE

- The forward resistance of the diode is graphically measured from the forward characteristic of the diode.

- DC resistance is always greater than a.c resistance of the diode (or) static resistance is always greater than dynamic resistance.

- under dc analysis, the ac signal voltage will be short circuited.

- under AC analysis :
  1. Biasing voltages are short circuited.
  2. The diode will be replaced by its dynamic resistance.

⇒ DYNAMIC RESISTANCE OF DIODE -

$$r = \frac{\eta V_T}{I_f} \quad \Omega$$

At room temp, if $I_f = 26\,mA$

then for Ge Diode $= 1\,\Omega$
and for Si Diode $= 2\,\Omega$

- when compare to germanium diode the dynamic resistance is more in the silicon diode.

$$r = \frac{\eta V_T}{I_f} = \frac{\eta \bar{k} T}{q I_f} \quad \Omega$$

⇒ DYNAMIC CONDUCTANCE (g) -

$$g = \frac{1}{r} \quad \mho \text{ or } S \text{ or } A/V$$

$$g = \frac{I_f}{\eta V_T} \quad \mho$$

$$\therefore \quad g \propto I_f$$

$$g = \frac{I_f}{\eta V_T} = \frac{q I_f}{\eta \bar{k} T} \quad \mho$$

⇒ BREAKDOWN VOLTAGE (V_{Br} or B_V) -

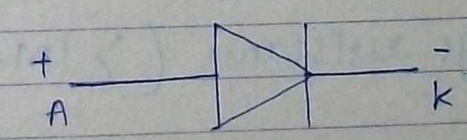
- It is manufacturer specification and it varies from device to device.

- In any type of PN-junction diode breakdown voltage is inversly prop. to doping.

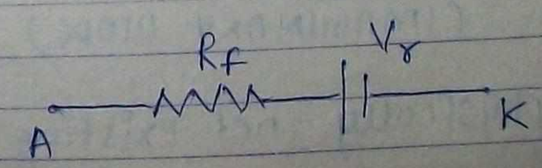
$$V_{Br} \propto \frac{1}{DOPING}$$

⇒ EQUIVALENT CIRCUT OF DIODE -

(1) WHEN DIODE IS FORWARD BIASED -

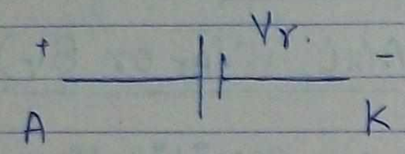


⇓



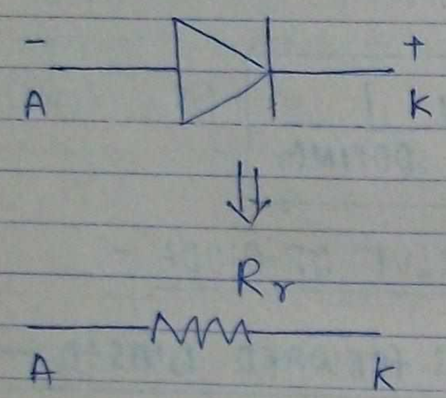
V_γ = CUTTING VOLT.
Typ. 0.2 V for Ge
0.7 V for Si

If forward resistance is neglected or not specified then.



- A forward biased diode can be replaced by its cutin voltage

(2) WHEN DIODE IS REVERSED BIASED -



R_r = very large resistance ($> 1M\Omega$).

⇒ **IDEAL DIODE** -

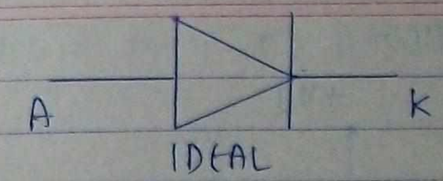
(PERFECT DIODE)

(OR)

(IMAGINARY DIODE)

ie physically not existing

SYMBOL -



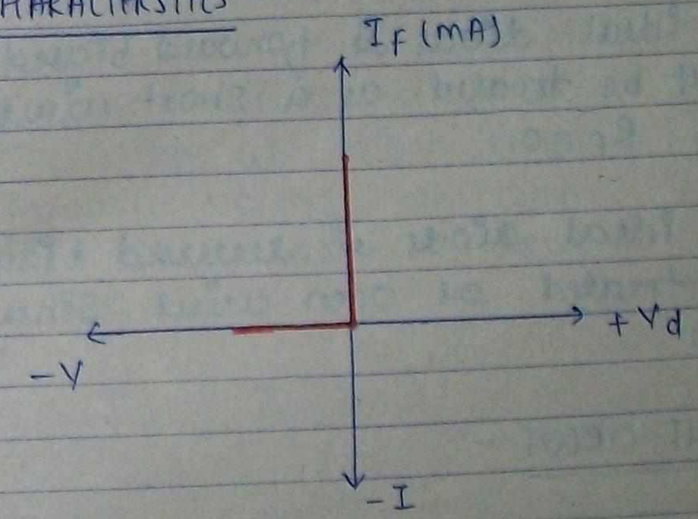
PROPERTIES -

$R_f = 0$

$R_r = \infty$

$V_\gamma = 0$

VI CHARACTERSTICS -



If IDEAL DIODE IS F.B -
Since $R_f = 0$
It is short circuit

$I \to max$

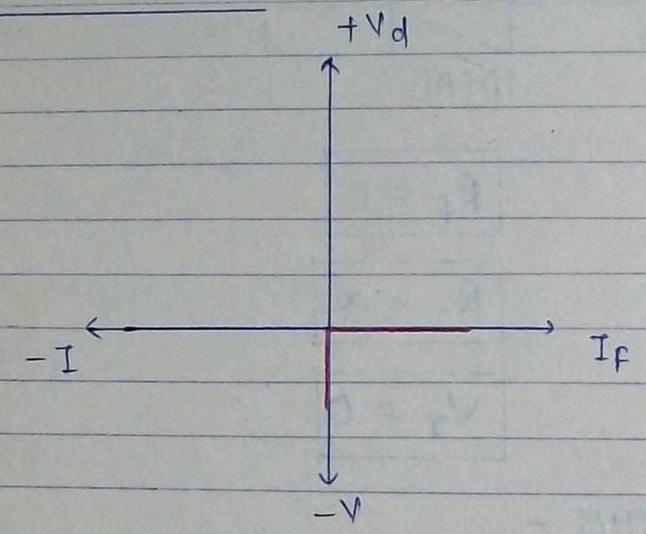
$V = 0$

If IDEAL DIODE IS R.B
Since $R_r = \infty$
It is open circuit.

$I \to 0$

$V = -ve$ & max.

IV CHARACTERSTIC -

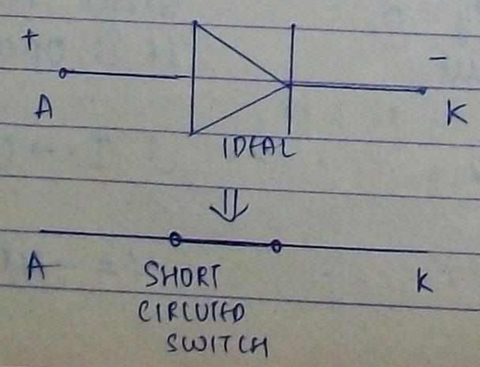


- when ideal diode is forward biased it will be treated as a short circuit since $R_f = 0$.

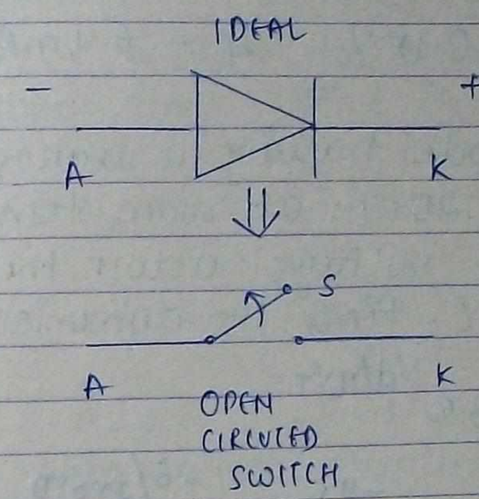
- when ideal diode is reversed biased it is treated as open circuit since $R_r = \infty$.

EQUIVALENT CIRCUT -

(1) WHEN IDEAL DIODE IS F.B -



(2) WHEN IDEAL DIODE IS R.B -



Qu. find the forward current of a Ge diode operating at room temp. with a forward voltage of 100mV across it. let the reverse saturation current is 20μA.

Soln:

$$I_f \cong I_0 e^{V_d/nV_T}$$

$$\simeq (20\times10^{-6})\, e^{(100\times10^{-3})/1\times26\times10^{-3}}$$

$$\cong \underline{\underline{0.936\ mA}}$$

Qu. Repeat the above problem when forward voltage across diode is 150mV.

Soln:

$$I_f \cong (20\times10^{-6})\, e^{(110/1\times26)} \cong \underline{\underline{6.4\ mA}}$$

NOTE - $V_d = 0.1\ V$ $I_f = 0.936\ mA$

$V_d = 0.15\ V$ $I_f = 6.4\ mA$

Qu. A Si diode having a leakage current of 20nA at room temp. let the forward voltage across the diode is 650 mV. find its dynamic resistance

Soln:

$$I_f = I_0 e^{V_d/\eta V_T}$$

$$I_f = (20\times10^{-9}) \times e^{26/2\times650}$$

$$= 5.367\ mA$$

$$r = \frac{\eta V_T}{I_f} = 9.688\ \Omega$$

Qu. A diode has a leakage current of 10 μA at certain temp. find its value when the temp is increased by 25 °C.

Soln:

$$I_{0(T_2)} = I_{0(T_1)} \left[2^{T_2 - T_1/10} \right]$$

$$= (10\times10^{-6}) \left[2^{25/10} \right]$$

$$= 56.56\ \mu A$$

Qu. A step graded Ge diode having $N_D = 500 N_A$ is subjected to acceptor impurities to the extent of 2 atoms for every 10^8 atoms at room temp. find its contact pot.? assume $V_T = 26\ mV$, $n_i = 2.5\times10^{13}\ atom/cm^3$
Total no. of atoms = $4.421\times10^{22}/cm^3$

Soln:

$$V_0 = V_T \log_e \left(\frac{N_A N_D}{n_i^2} \right)$$

$$n \simeq N_A = \text{Total atom}/cm^3 \times \text{Impurity ratio}$$

$$= 4.421\times10^{22} \times \frac{2}{10^8}$$

$$= 8.842\times10^{14}\ atom/cm^3$$

$$N_D = 500 \times N_A = 4421\times10^{14}\ atom/cm^3$$

$$V_0 = (26\times10^{-3}) \log_e \left[\frac{8.842\times10^{14} \times 4421\times10^{14}}{(2.5\times10^{13})^2} \right]$$

$$= 0.347\ Volts \simeq 347\ mV$$

Qu. A step graded Si diode having $N_D = 500 N_A$ is subjected to acceptor impurities of 2:108 at room temp. find contact potential, $n_i = 1.5\times10^{10}\ atom/cm^3$
no of atoms = $5\times10^{22}/cm^3$

ANS (739 mV)

Sol^n: $n \simeq N_A = 5\times10^{22} \times \frac{2}{10^8} = 10\times10^{14} / cm^3$

$N_D = 500\, N_A$

$= 5000\times10^{14} / cm^3$

$V_0 = V_T \log_e \left(\frac{N_A N_D}{n_i^2}\right)$

$= (26\times10^{-3}) \log_e \left(\frac{5000\times10^{14}\times10\times10^{14}}{(1.5\times10^{10})^2}\right)$

$= 739\times10^{-3} = 739\, mV$

Que. A si diode indicates a forward current of 2mA and 10mA when forward voltage across the diode is 0.6 V and 0.7 V resp. estimate the operating temp. of the diode junction?

Sol^n:

$I_f \simeq I_0 e^{V_d/nV_T}$

but $V_T = T/11600$

$I_f = I_0 e^{\frac{11600 V_d}{nT}}$

$2 = I_0 e^{\frac{11600\times0.6}{2T}}$ — (1)

$10 = I_0 e^{\frac{11600\times0.7}{2T}}$

(1)/(2) $\frac{2}{10} = e^{\frac{1}{2T}(11600)(0.6-0.7)}$

$\log(1/5) = \frac{11600}{2T}(-0.1)$

$T = +360.37\, K \simeq 360\, K$

Que. A PN junction in series with a 100Ω resistor is f.B. so that a current of 100mA flows, if the voltage across this combination is instantly reversed to 10V at time t=0, the current that flows through the diode at t=0 is approx —.

(1) 0 mA (2) 50 mA

(3) 100 mA (4) 200 mA.

Sol^n: At time t=0, the diode is suddenly reversed biased and it will take certain ~~dio~~ time for diode to become R.B.

At time t=0, the diode is still under f.B and the forward current will be 100 mA

Que. A forward biased Si diode when carrying negligible current has a voltage drop of 0.64 V, when the current is 1 Amp, it dissipates 1 W the on resistance of the diode is :

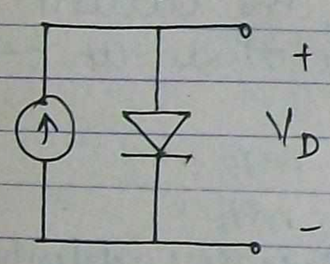
(1) 0.36 Ω (2) 0.64 Ω
(3) 0.72 Ω (4) 1 Ω

Soln:

$$P = I^2 R_{ON}$$

$$R_{ON} = \frac{1}{(1)^2} = 1$$

Que. In a circuit given below, Si diode is carrying a current of 1mA. Then the temperature of the diode is 20°C, V_D is found to be 700 mV. If the temp increases to 40°C, V_D becomes ___



(1) 740 mV (2) 660 mV (3) 680 mV (4) 780 mV

Soln:

$$I_0(40) = 700 \left[2^{20/10}\right] = 2800 \text{ mV}$$

wrong approach.

for 1°C, $V_D \downarrow$ by 2mV

Temp changes from 20° to 40°C

$\Delta T = 20°C$ $\Delta V_D = \Delta T \times 2mV/°C$

$= 20°C \times 2mV/°C$

$= 40 mV$

$V_D = 700mV - 40mV$

$= 660 mV$

Que. At 300K, for a diode current of 1mA, a certain Ge diode requires a forward voltage of 0.1435 V across it, whereas a certain Si diode requires 0.718 V across it, under the condn given above find $\frac{I_0(Ge)}{I_0(Si)}$ ratio.

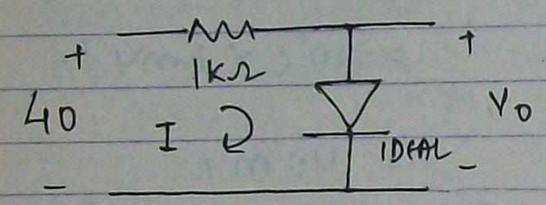
Soln:

$$I_0(Ge)\, e^{0.1435/1\times26\times10^{-3}} = I_0(Si)\, e^{0.718/2\times26\times10^{-3}}$$

$$\frac{I_0(Ge)}{I_0(Si)} \simeq 3978$$

⇒ SIMPLE DIODE CIRCUITS –

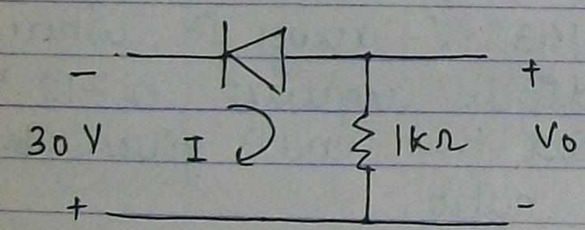
Qu. find I and V_0 :



Sol^n: $I = \frac{40}{1\times10^3} = \underline{\underline{40\,mA}}$

$V_0 = \underline{\underline{0}}$ short circuited.

Qu. find I and V_0 :

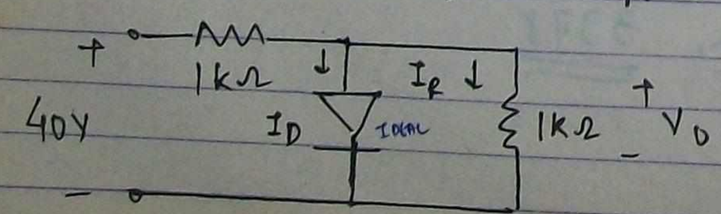


Sol^n: $V_0 = \underline{\underline{-30\,V}}$.

$I = \frac{-30}{1k} = \underline{\underline{-30\,mA}}$

assumed direction is wrong.

Qu. find V_0, I, I_D and I_R :

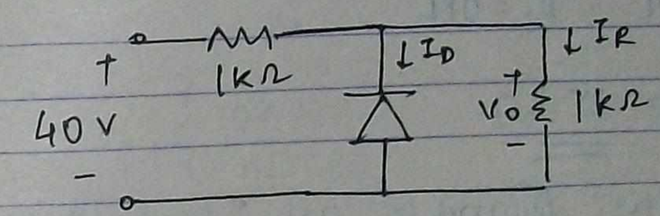


Sol^n: $V_0 = \underline{\underline{0}}$

$I_D = \frac{40}{1\times10^3} = 40\,mA$

$I_R = 0$, $I = I_D = \underline{\underline{40\,mA}}$

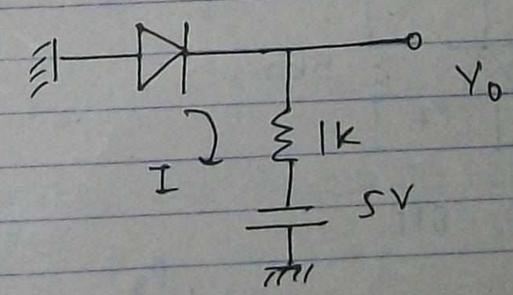
Qu. find same in:



Sol^n: $I_D = 0$, $I_R = I = \frac{40}{2\times10^3} = 20\,mA$

$V_0 = I_R \times 1k = \underline{\underline{20\,V}}$

Qu. find I and V_0 :

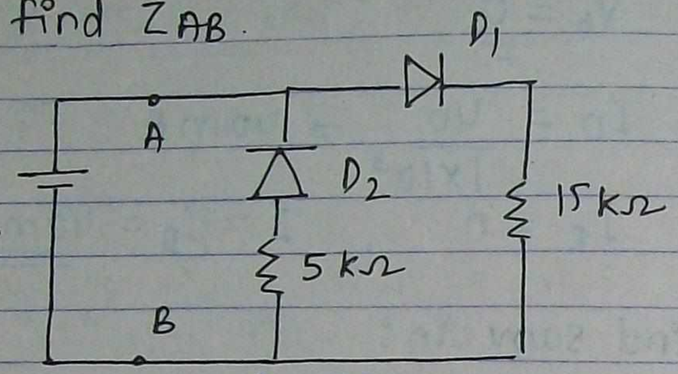


Sol^n: $I = \frac{5}{10^3} = 5\,mA$

$V_0 = -5\,mA(1k) + 5$

$= \underline{\underline{0}}$

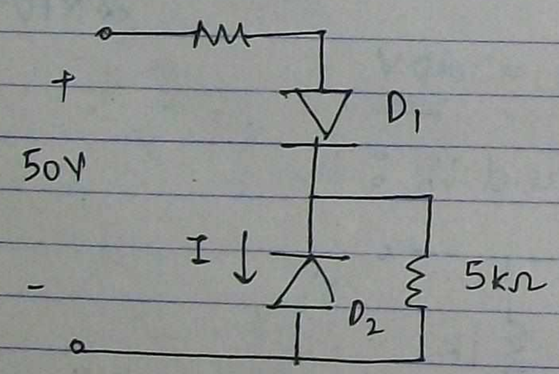
Que. find Z_{AB}.



Sol^n: D_1 = ON D_2 = Off

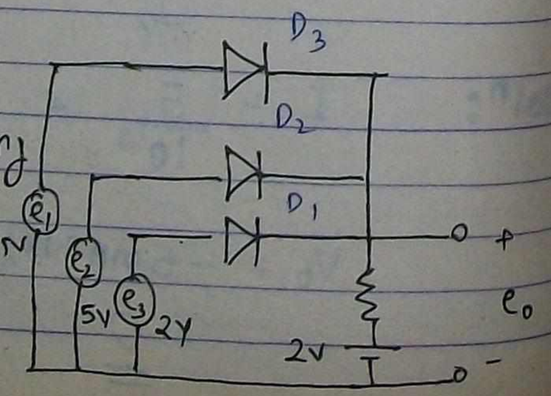
Z_{AB} = 15 kΩ

Que. Assuming D_1 and D_2 are ideal diode find the current I in circuit:

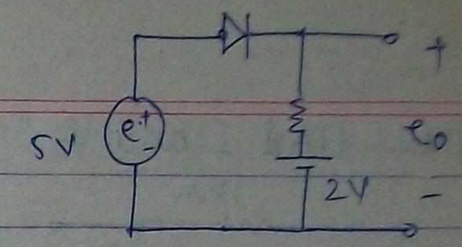


Soln: ZERO. D_2 = Off

Que. find which diode is conducting in circuit given below and also calculate e_o (o/p voltage)

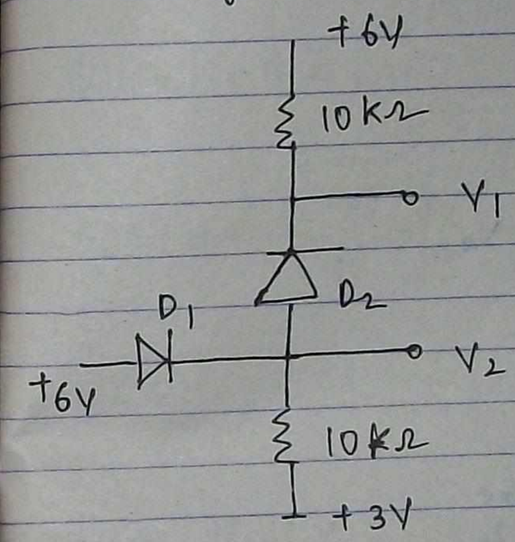


Sol^n: Predominant by 5V



D_2 and $V_o = e_o$ = 5V

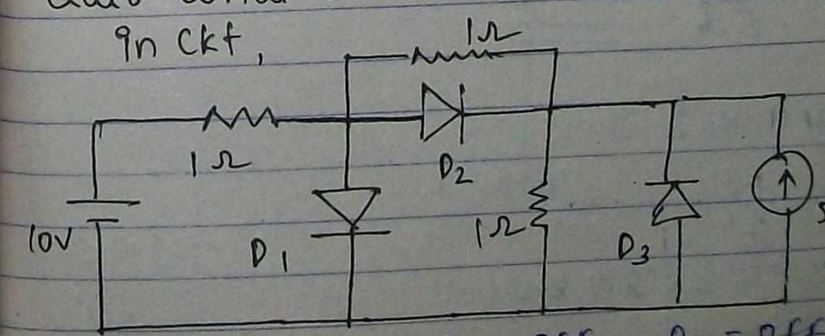
Que. The voltages at V_1 and V_2 of the arrangement given in fig will be ——.



(1) 6V & 5.4V
(2) 5.4V & 6V
(3) 3V & 5.4V
(4) 6V & 6V.

Soln: D_2 = Short.

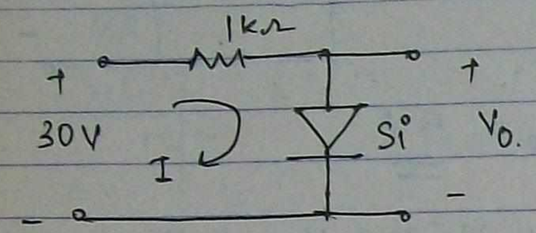
Que. what are the states of the three ideal diodes in ckt,



	D_1	D_2	D_3
(1)	OFF	ON	ON
(2)	ON	OFF	ON
(3)	OFF	ON	OFF
(4)	ON	OFF	OFF

Soln: D_1 = ON D_2 = OFF D_3 = OFF

Qu. find I and V_0:

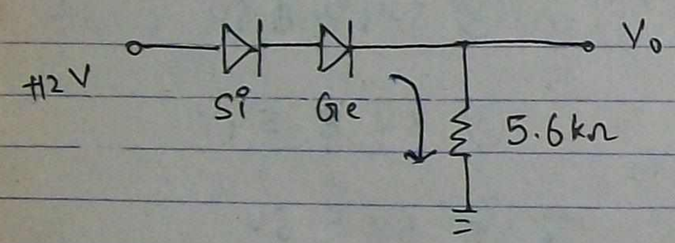


Sol^n:

$$I = \frac{30-0.7}{1k\Omega} = 29.3\,mA$$

$$V_0 = 0.7\,V$$

Qu. find I and V_0:

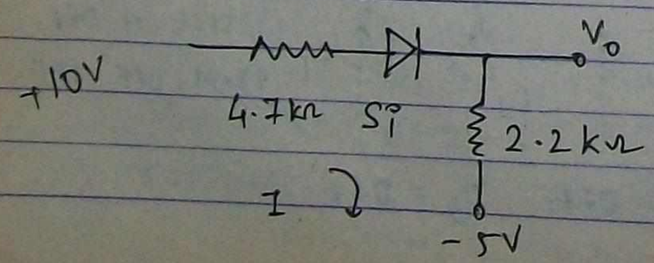


Sol^n:

$$V_0 = 12 - V_{Si} - V_{Ge}$$
$$= 12 - 0.7 - 0.2$$
$$= 11.1$$

$$I = \frac{11.1}{5.6} = 1.98\,mA$$

Qu. find I and V_0:

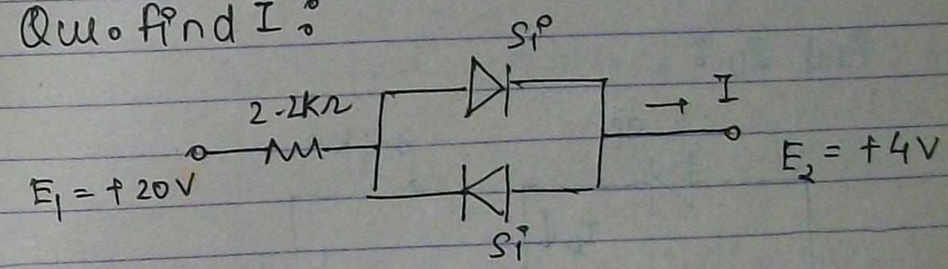


Sol^n: $I \geq 10 = 4.7\,I + 0.7 + 2.2\,I - 5$

$$I = \frac{15-0.7}{6.9} = 2.07\,mA$$

$$V_0 = +2.2 \times 2.07 - 5$$
$$= -0.446$$

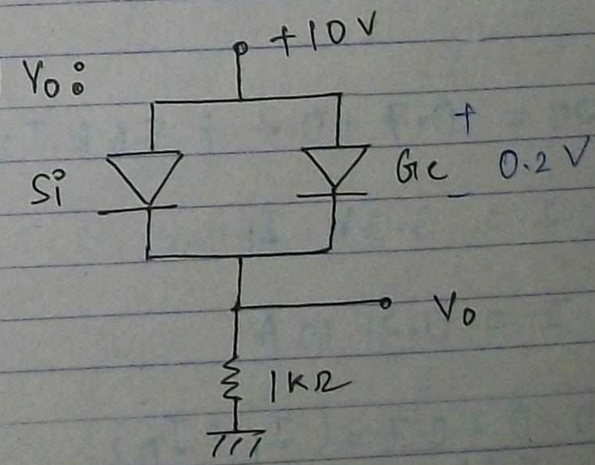
Qu. find I:



Sol^n:

$$I = \frac{20-4-0.7}{2.2k\Omega} = 6.95\,mA$$

Qu. find V_0:



Sol^n:

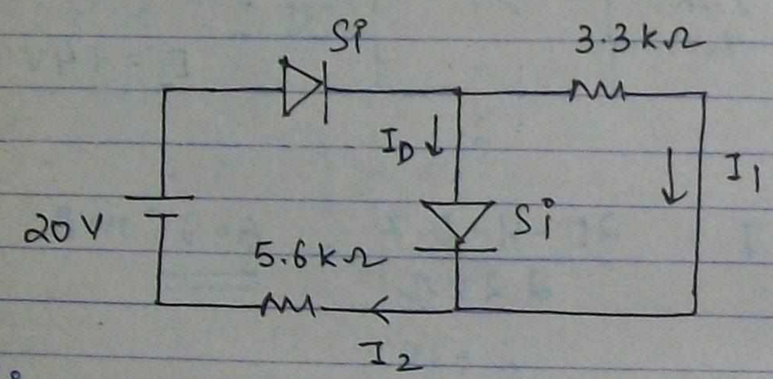
$$V_0 = 10 - 0.2 = 9.8\,V$$

Si, diode is forward biased & non conducting

Both Ge and Si diode are F.B and due to smaller cutin voltage, Ge diode will enter into conduction and O/P voltage is 9.8 V.

The Si diode is forward biased and is non conducting & also it will never get the chance to conduct.

Que. find I_D :



Soln:

$$20 = 0.7 + 0.7 + 5.6k\, I_2$$

$$0.7 = 3.3k \cdot I_1$$

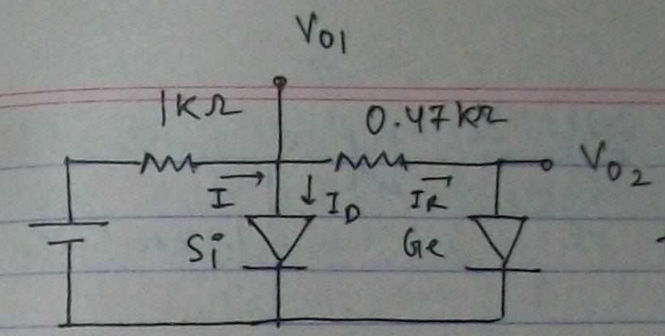
$$I_1 = 0.21 \text{ mA}$$

$$\frac{20 - 0.7 - 0.7}{5.6k} = (I_1 + I_D)$$

$$I_D = 3.321 - 0.21$$

$$I_D = \underline{\underline{3.11 \text{ mA}}}$$

Que.



find V_{01} & V_{02}

Soln: $V_{01} = \underline{\underline{0.7}}$ $V_{02} = \underline{\underline{0.2}}$

Que. Previous problem find I, I_D, I_R.

Soln:

$$20 = 1k\, I + 0.47k\, I_R + 0.2$$

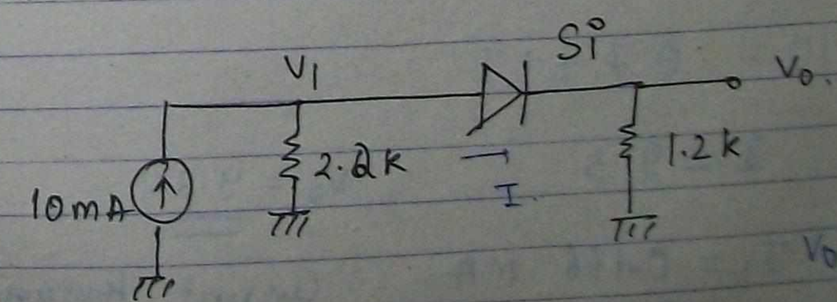
$$20 = 1.47k\, I_R + 0.2 + 1k\, I_D$$

$$I_R = \frac{0.7 - 0.2}{0.47k} = \underline{\underline{1.06 \text{ mA}}}$$

$$I = \frac{20 - 0.7}{1k} = \underline{\underline{19.3 \text{ mA}}}$$

$$I_D = \underline{\underline{18.24 \text{ mA}}}$$

Que. find I, V_1 and V_0 :

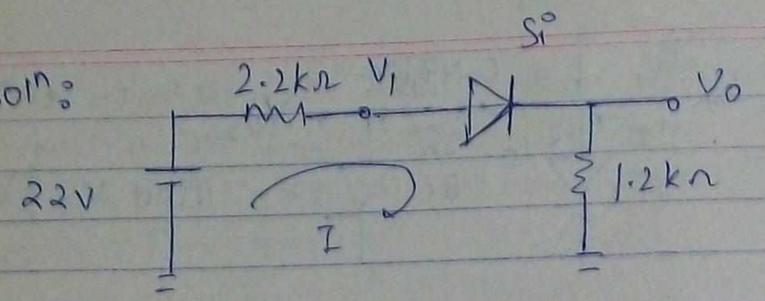


$V_0 = \underline{\underline{7.769}}$

Soln $I = \frac{2.2}{3.4} \times 10 = \underline{\underline{6.47 \text{ mA}}}$

$V_1 = 7.766$

Sol^n:

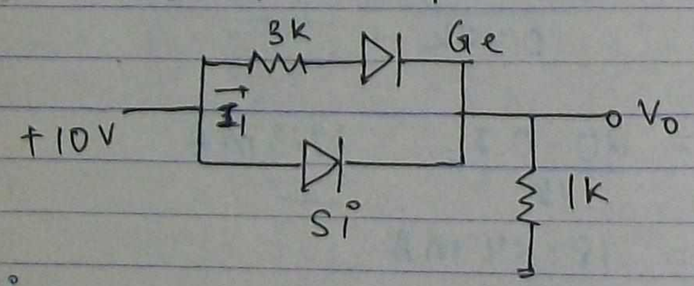


$$I = \frac{22 - 0.7}{2.2 + 1.2} = 6.26\,mA$$

$$V_1 = 22 - I(2.2k) = 8.21\,V$$

$$V_0 = V_1 - V_{r\,Si}$$
$$= 8.21 - 0.7 = 7.51\,V$$

Que. find V_0 and I_1



Sol^n:

$$10 = 3I_1 + 0.2 + 1I$$

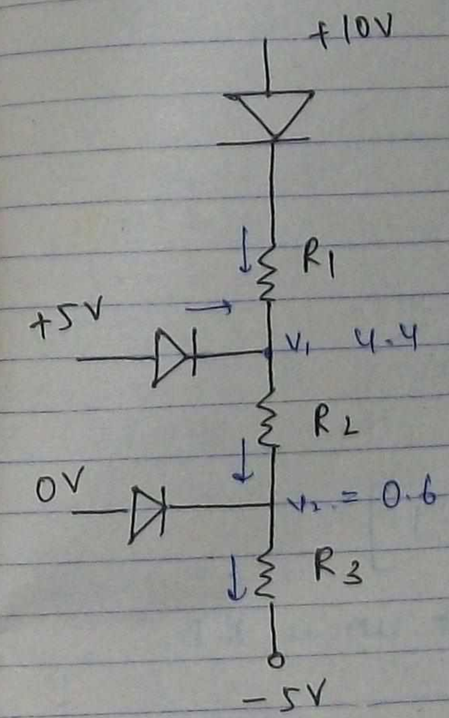
$$10 = 0.7 + 1I$$

$$I = 9.3 \quad , \quad V_0 = 9.3\,V$$

$$I_1 = 0.166\,mA$$

Current through Si = 9.133 mA

Que. The cutin voltage for each diode is 0.6V and each diode current is 0.5 mA find value of R_1, R_2, R_3



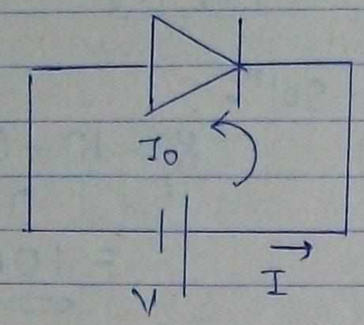
Sol^n:

$$R_1 = \frac{10 - 0.6 - 4.4}{0.5} = 10\,k\Omega$$

$$R_2 = \frac{4.4 + 0.6}{1} = 5\,k\Omega$$

$$R_3 = \frac{5 - 0.6}{1.5} = 2.93\,k\Omega$$

⇒ EQUATION FOR CURRENT WHEN DIODE IS REVERSED BIASED -



$$\boxed{I = I_0} \quad \text{Amp.}$$

since,

$$I_f = I_0 \left[e^{V_d/\eta V_T} - 1 \right]$$

but according to circuit under R.B.

$$\boxed{I = -I_0 \left[e^{-V/\eta V_T} - 1 \right]} \quad \text{Amp.}$$

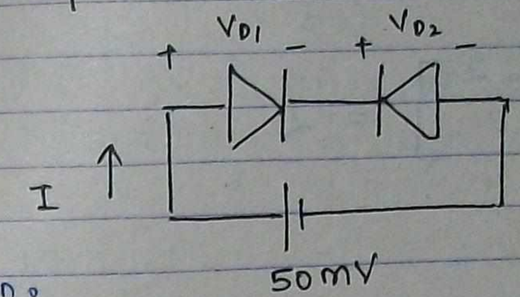
$$\boxed{I \simeq I_0} \quad \text{Amp}$$

Since, let Ge, $\eta = 1$, $V_T = 26\,mV$

$V = 5V$

$$e^{-5/26\times10^{-3}} \simeq 3.03 \times 10^{-84}$$

Que. The circuit given below consist of two identical diodes each having a utility factor of unity. ($\eta = 1$) assume $V_T = 25\,mV$. find the value of V_{D_1} & V_{D_2}.



Soln:

D1 is forward biased and D_2 is reverse biased, hence the forward current in D_1 will flow as reverse current in D_2.

for D_1:

$$I_f = I_0 \left[e^{V_{D1}/\eta V_T} - 1 \right]$$

for D_2:

$$I = I_0 = -I_0 \left[e^{-V_{D2}/\eta V_T} - 1 \right]$$

from both equations:

$$I_0 \left[e^{V_{D1}/\eta V_T} - 1 \right] = -I_0 \left[e^{-V_{D2}/\eta V_T} - 1 \right]$$

$$e^{V_{D1}/\eta V_T} + e^{-V_{D2}/\eta V_T} = 2$$

but $V_{D1} + V_{D2} = 50mV$

$V_{D2} = 50mV - V_{D1}$

$$e^{V_{D_1}/\eta V_T} + e^{-(50-V_{D_2})/\eta V_T} = 2$$

$$e^{V_{D_1}/\eta V_T} + e^{-50mV/\eta V_T} \; e^{+V_{D_1}/\eta V_T} = 2.$$

$$e^{V_{D_1}/\eta V_T}\left[1+e^{-2}\right] = 2$$

$$e^{V_{D_1}/\eta V_T} = \frac{2}{1+e^{-2}}$$

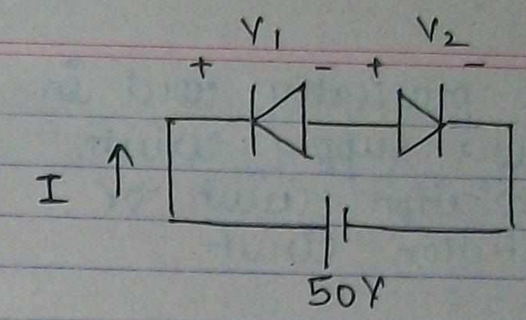
$$V_{D_1} = \eta V_T \log_e\left[\frac{2}{1+e^{-2}}\right]$$

$$V_{D_1} = 1\times 26\,mV \log_e\left(\frac{2}{1+e^{-2}}\right)$$

$$V_{D_1} = \underline{\underline{14.15\,mV}}$$

$$V_{D_2} = 50 - 14.15 \simeq \underline{\underline{35.85\,mV}}$$

Que. In the circuit given below the two identical Ge diodes are connected, let $V_T = 25\,mV$. find the values of V_1 and V_2



Soln: D_1 is reversed bias and D_2 is forward biased and therefore the leakage current of D_1 will flows as forward current in D_2.

for D_1:

$$I = I_0$$

for D_2:

$$I = I_f = I_0\left[e^{V_2/\eta V_T} - 1\right]$$

from both eqn:

$$I_0 = I_0\left[e^{V_2/\eta V_T} - 1\right]$$

$$e^{V_2/\eta V_T} = 2$$

$$V_2 = \eta V_T \log_e 2$$

$$V_2 = 1\times 26\times 10^{-3} \times \log_e 2 = \underline{\underline{17.32\,mV}}$$

$$V_1 = 50V - V_2$$

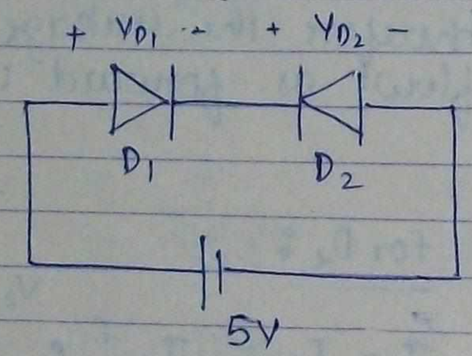
$$V_1 = \underline{\underline{49.98\,V}}$$

24/7/11

NOTE - Above circuits are pratically used in designing of power supply circuits as overload protection circuit or short circuit protection circuit

Que. P-18 Q1. (conventional)

Soln:



$V_T = 25\,mV$

for D_1:

$$I = I_0\left[e^{V_{D_1}/\eta V_T} - 1\right]$$

for D_2:

$$I = -I_0\left[e^{-V_{D_2}/\eta V_T} - 1\right]$$

$$e^{V_{D_1}/\eta V_T} + e^{-V_{D_2}/\eta V_T} = 2$$

$$V_{D_1} + V_{D_2} = 5V \qquad V_{D_2} = 5 - V_{D_1}$$

$$e^{V_{D_1}/\eta V_T} + e^{-5/\eta V_T} \cdot e^{V_{D_1}/\eta V_T} = 2$$

$$e^{V_{D_1}/\eta V_T}\left(1 + e^{-5/25\times 2\times 10^{-3}}\right) = 2$$

$$e^{V_{D_1}/2\times 25\times 10^{-3}} = 2$$

$V_{D_1} = 34.325\,mV$

$V_{D_2} = 4.965\,V$

Que 2. conventional.

Soln: $V_T = 26\,mV$ $\quad N_A = 10^{18}/cm^3$

$N_D = 10^{15}/cm^3$ $\quad n_i = 1.5\times 10^{10}$

$$V_0 = V_T \log_e\left(\frac{N_A N_D}{n_i^2}\right)$$

$$= 0.757\,V \quad \text{or} \quad 757\,mV$$

Que 3. conventional.

Soln: $N_A = 10^{23}/m^3$ $\quad N_D = 10^{21}/m^3$

$n_i = 1.5\times 10^{16}/m^3$

$\varepsilon_r = 11.8$

$$V_0 = V_T \log_e\left(\frac{N_A N_D}{n_i^2}\right)$$

$$= 697\,mV$$

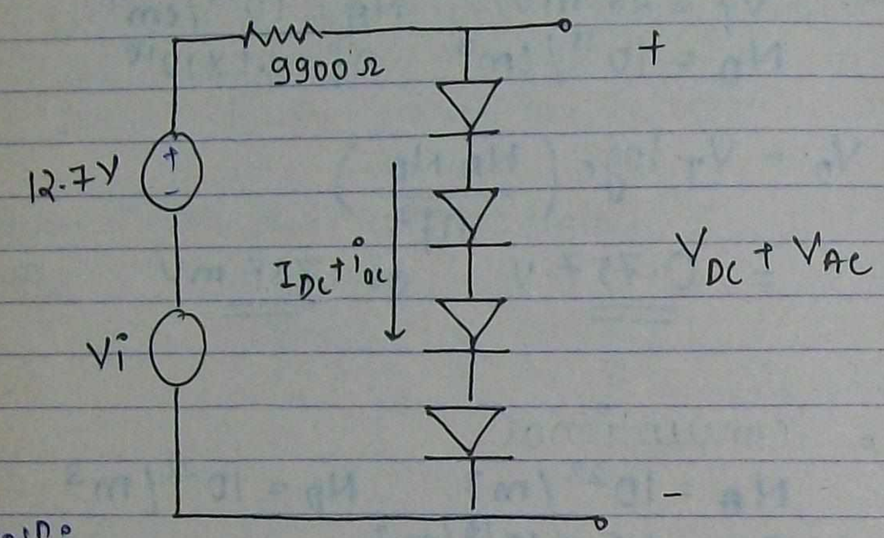
$$w = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0}$$

$$\varepsilon = \varepsilon_0 \varepsilon_r$$

$$w = \sqrt{\frac{2\times 8.85\times 10^{-12}\times 11.8}{1.6\times 10^{-19}}\left(\frac{1}{10^{23}} + \frac{1}{10^{21}}\right) 0.697}$$

$$w = 0.958\,\mu m.$$

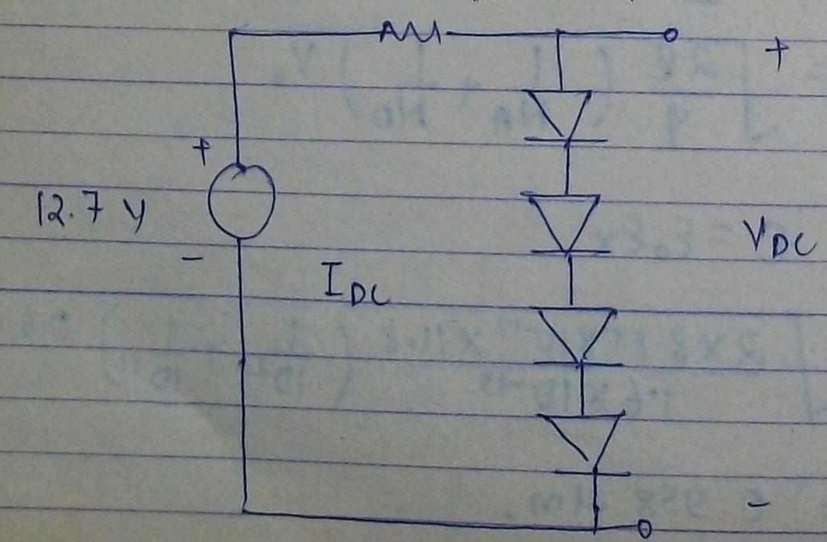
Que. P-16 Q. 22, 23



Soln:

for dc current we apply dc analysis i.e the signal voltage in the circuit will be reduced to zero. ($V_i = 0$)

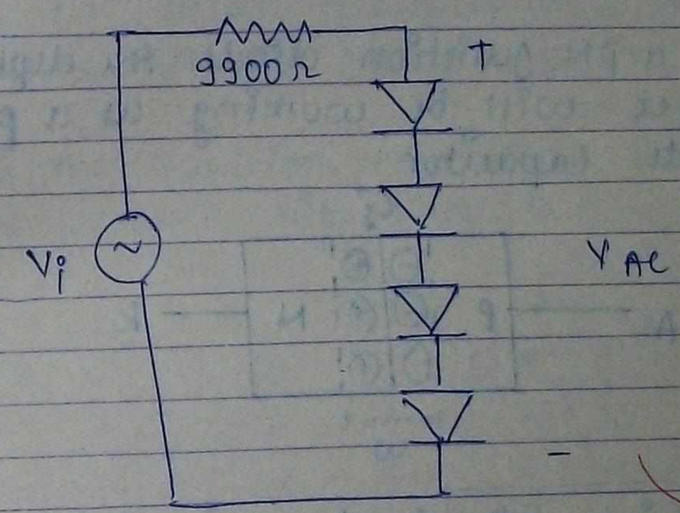
(*) In the above circuit the diode are connected as a STRING.



$$I_{DC} = \frac{12.7 - (4 \times 0.7)}{9900} = \underline{\underline{1mA}}$$

under ac analysis:

1. biasing voltages are kept zero.
2. diode will be replaced by its dynamic resistance.



$$r = \frac{\eta V_T}{I_f} = \frac{\eta V_T}{I_D}$$

Since diode is not specified let $\eta = 1$

$$r = \frac{1 \times 25 \times 10^{-3}}{1 \times 10^{-3}} = \underline{\underline{25\ \Omega}}$$

Dynamic resistance of four diode $= 4 \times 25 =$
$= \underline{\underline{100\ \Omega}}$

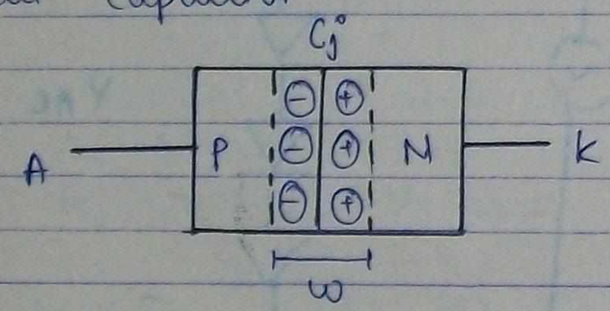
$$V_{AC} = \frac{V_P(100)}{9900+100} = \frac{100mV(100)}{10,000}$$

$$= 1mV$$

$$V_{AC} = 1\cos(\omega t)\ mV$$

⇒ JUNCTION CAPACITANCE (C_J) –

- In a PN junction diode the depletion layer will be working as a parallel plate capacitor



$$C_j = \frac{\varepsilon A}{w} \text{ farad.} \qquad \varepsilon = \varepsilon_0 \varepsilon_r$$

$$C_j \propto \frac{1}{w} \qquad C_j \Rightarrow pf \text{ ie } 10^{-12} f$$

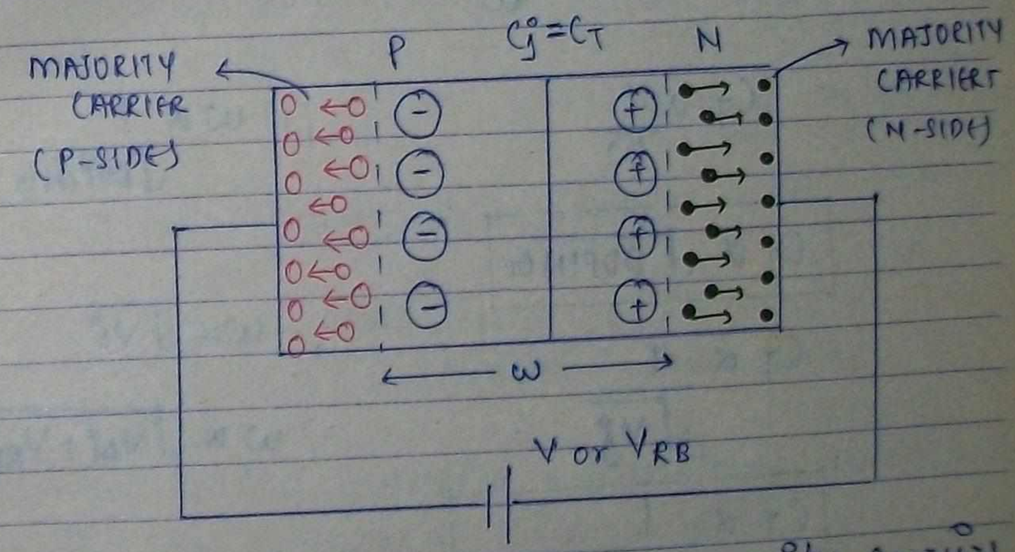
C_j → C_T (TRANSITION CAPACITANCE)
C_j → C_D (DIFFUSION CAPACITANCE)

- when diode is open circuited there will be C_T and C_D in the device and when biasing is applied, one of the capacitance will be dominating.

① TRANSITION CAPACITANCE (C_T) –

- It is also called depletion layer capacitance or space charge capacitance.

- C_T is the junction capacitance dominated in the reverse biased diode.



- C_T is due to storage of majority carriers in the reversed biased diode.

- for better performance of the diode at high frequencies, the C_T value must be very small.

TYP. VALUE - 3 PF BJT
5 PF DIODE

- Typical value $C_T = 3\,pF$ for BJT
  $C_T = 5\,pF$ for DIODE
  BJT gives better performance than diode in high frequencies.

- The property of C_T is used in designing of varactor diode.

- In a reverse biased diode, the transition capacitance:

$$C_j = C_T = \frac{\varepsilon A}{W}$$

$C_T \propto \frac{1}{W}$, $W \propto \frac{1}{\sqrt{DOPING}}$

$\boxed{C_T \propto \sqrt{DOPING}}$

$C_T \propto \frac{1}{\sqrt{V_j}}$, $W \propto \sqrt{V_j}$

$\boxed{C_T \propto \frac{1}{\sqrt{V_{bi} + V_{RB}}}}$, $W \propto \sqrt{V_{bi} + V_{RB}}$

$\boxed{C_T \propto \frac{1}{\sqrt{V_{RB}}}}$, $W \propto \sqrt{V_{RB}}$.

- In a reverse biased diode, the transition capacitance C_T

$$\boxed{C_T \propto V^{-n}}$$

where V is the applied reverse voltage or reverse biased voltage and 'n' is a constant and

$n = 1/2$ for step graded diode (P^+N, PN^+) or abrupt PN junction diode

$n = 1/3$ for linear graded diode (P^+N^+) $N_A = N_D$

$n = 1/2.5$ for diffused PN junction diode (IC FORM)

n = grading coefficient.

(2) DIFFUSION CAPACITANCE (C_D) - (STORAGE CAPACITANCE)

- C_D is the junction capacitance dominated in the forward biased diode.

- C_D is responsible for the storage of minority carriers in the forward biased diode.

$$\boxed{C_j = C_D = \frac{\varepsilon A}{W}}$$

$$C_D \propto \frac{1}{W}$$

$$\boxed{C_D \propto \sqrt{\text{DOPING}}} \quad , \quad W \propto \frac{1}{\sqrt{\text{DOPING}}}$$

$$\boxed{C_D \propto \sqrt{\text{FORWARD BIASED}}} \quad , \quad W \propto \frac{1}{\sqrt{\text{F.B.}}}$$

- The performance of a diode or BJT is very badly affected due to the presence of C_D.

- The high frequency operation of the diode is limited by C_D.

- C_D is a high frequency parameter ie it will appear in the device only during high frequency operation.

$$\boxed{C_D = \tau \cdot g} \quad \text{farad.}$$

τ is mean life time of minority carrier
g is dynamic conductance.
r is dynamic resistance.

$$C_D = \frac{\tau}{r} \quad \text{farad}$$

(A) $$\boxed{C_D = \frac{\tau \cdot I_f}{\eta V_T}} \qquad \left(r = \frac{\eta V_T}{I_f}\right)$$

(A) $$\boxed{C_D \propto I_f}$$

- Diffusion capacitance linearly increases with forward current.

but $I_f = I_0 \left[e^{V_d/\eta V_T} - 1 \right] \simeq I_0 e^{V_d/\eta V_T}$

$$\boxed{C_D = \frac{\tau \cdot I_0 e^{V_d/\eta V_T}}{\eta V_T}}$$

- Diffusion capacitance exponentially increases with forward voltage across the diode.

⇒ <u>MEAN LIFE TIME OF MINORITY CARRIER (τ)</u> -
(CARRIER LIFE TIME)
OR
(AVERAGE LIFE TIME)

τ is in range from μsec to nsec.

$$\boxed{\tau = \frac{C_D}{g} = C_D \cdot r = \frac{\eta V_T C_D}{I_f}}$$ sec.

- The mean life time of minority carriers is approximately equal to the time constant of the diode.

⇒ **DERIVE AN EQUATION FOR TRANSITION CAP. (C_T)-**

- Transition capacitance will appear in the diode when operated under reverse biased
- It is the junction capacitance of the reverse biased diode.

$$C_T = C_j = \frac{\varepsilon A}{W} \quad \text{farad}$$

but

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0+V_{RB})}$$

$$C_j = C_T = \frac{\varepsilon A}{\sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0+V_{RB})}}$$

$$C_j = C_T = \frac{A}{\sqrt{\frac{2}{q\varepsilon}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0+V_{RB})}}$$

$$C_j = C_T = \frac{A}{\sqrt{\frac{2}{q\varepsilon}\left(\frac{N_A+N_D}{N_AN_D}\right)V_0\left(1+\frac{V_{RB}}{V_0}\right)}}$$

$$C_j = C_T = \frac{A\sqrt{\frac{q\varepsilon}{2}\left(\frac{N_AN_D}{N_A+N_D}\right)\frac{1}{V_0}}}{\sqrt{1+\frac{V_{RB}}{V_0}}}$$

Suppose if reverse biased voltage is zero. $V_{RB}=0$

$$\boxed{\underset{\substack{\downarrow \\ C_{j0}}}{C_j} \equiv C_T \equiv A\sqrt{\frac{q\varepsilon}{2V_0}\left(\frac{N_AN_D}{N_A+N_D}\right)}} \quad \text{farad}$$

- C_{j0} is the value of junction capacitance when reversed biased voltage is kept zero.

$$\frac{C_{j0}}{A} = \sqrt{\frac{q\varepsilon}{2V_0}\left(\frac{N_AN_D}{N_A+N_D}\right)} \quad \text{farad}/m^2$$

Thus,

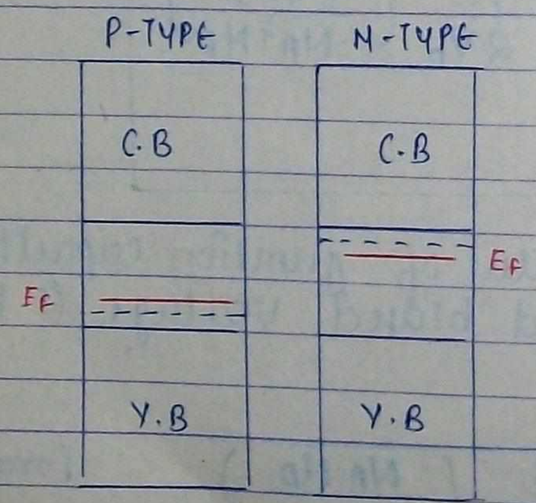
$$C_j = \frac{C_{j0}}{\left[1 + \frac{V_{RB}}{V_0}\right]^{1/2}} \quad \text{farad}$$

The above equation of the transition capacitance can be generalised by:

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_{RB}}{V_0}\right)^{m}} \quad \text{farad.}$$

where m = grading coefficient.

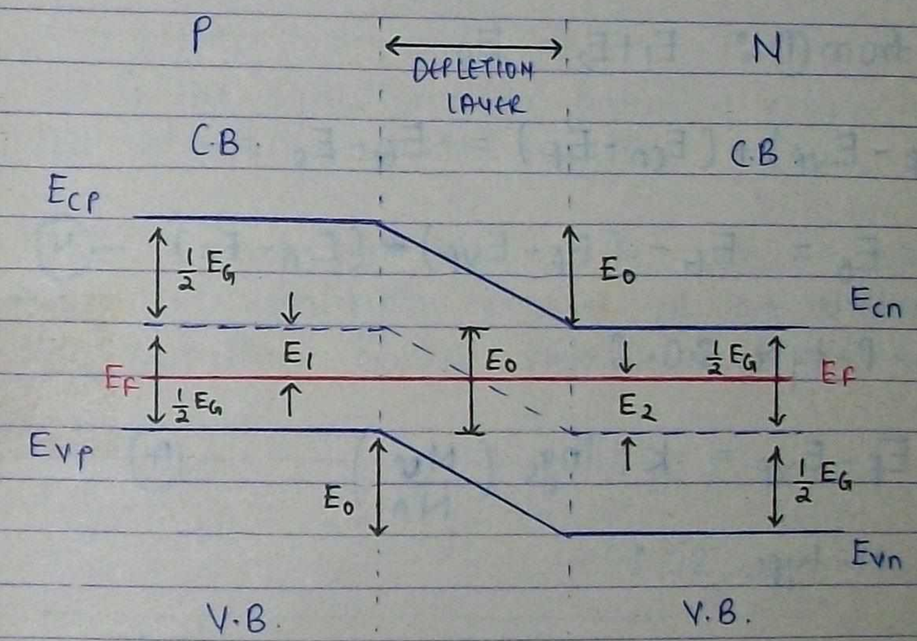
⇒ **DERIVE AN EQUATION FOR CONTACT POTENTIAL OF THE DIODE UNDER OPEN CIRCUT CONDITION-**



- In the P type semiconductor at room temp. the fermi level will be existing just above the acceptor energy level.

- In N type semiconductor the fermi level will be existing just below the donor energy level.

- In open circuit PN junction, the fermi level will maintain a straight line as given below:



- In the above diagram, E_0 is potential energy of the electrons at the junction.

- from the given diagram:

$$E_0 \equiv E_{cp} - E_{cn} \equiv E_{vp} - E_{vn} \equiv E_1 + E_2 \quad -(1)$$

$$E_f - E_{vp} = \frac{1}{2} E_G - E_1 \quad -(2)$$

$$E_{cn} - E_f = \frac{1}{2} E_G - E_2 \quad -(3)$$

adding eq (2) and (3):

$$(E_f - E_{vp}) + (E_{cn} - E_f) = E_G - (E_1 + E_2)$$

from (1): $E_1 + E_2 = E_0$

$$(E_f - E_{vp}) + (E_{cn} - E_f) = E_G - E_0$$

$$E_0 = E_G - (E_f - E_{vp}) + (E_{cn} - E_f) \quad -(4)$$

in P-type S.C.:

$$E_f - E_{vp} = kT \log_e \left(\frac{N_v}{N_A}\right) \quad -(A)$$

in N-type SC:

$$E_{cn} - E_f = kT \log_e \left(\frac{N_c}{N_D}\right) \quad -(B)$$

In a semiconductor:

$$E_G = kT \log_e \left(\frac{N_c N_v}{n_i^2}\right) \quad -(C)$$

Subsituting eq (A), (B) and (C) in eq (4):

$$E_0 = kT \log_e \frac{N_c N_v}{n_i^2} - kT \log_e \frac{N_v}{N_A} - kT \log_e \frac{N_c}{N_D}$$

$$E_0 = kT \log_e \left[\frac{N_c N_v}{n_i^2} \times \frac{N_A}{N_v} \times \frac{N_D}{N_c}\right]$$

$$\boxed{E_0 = kT \log_e \frac{N_A N_D}{n_i^2}} \quad eV.$$

- It is the equation for potential energy of the electrons at the junction.

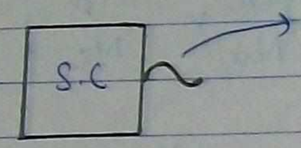
- The contact potential of the diode is numerically equal to Potential energy of the electrons at the junction when expressed in volts.

$$\boxed{V_0 = V_{bi} = V_T \log_e \frac{N_A N_D}{n_i^2}} \quad \text{volt}$$

SPECIAL DIODES & OPTOELECTRONIC DEVICES

⇒ POINT CONTACT DIODE -

(METAL - S.C. JUNCTION DIODE)



TUNGSTEN WIRE IN MICRONS & IS CALLED CAT WHISKER

- The least value of junction capacitance is obtained with point contact diode.
- It is the earliest diode or first diode (100 years old).
- Since contact area is very small, C_j will be negligible

$$C_j = \frac{\varepsilon A}{W}$$

- It can work as an rectifier.

⇒ VARACTOR DIODE (VD) -

- Linear graded diode.
- PRINCIPLE -

TRANSITION CAP. (C_T)

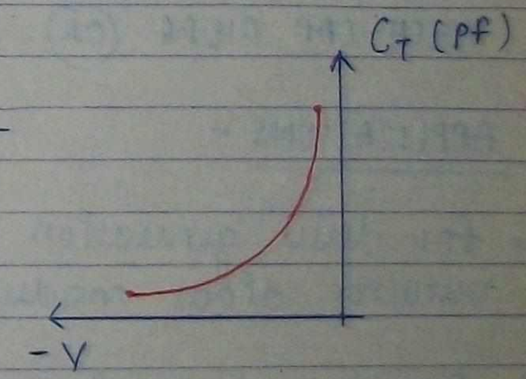
- Always operated under reversed biased.

$$C_T \propto V^{-n}$$ when $n = 1/3$ for VD.

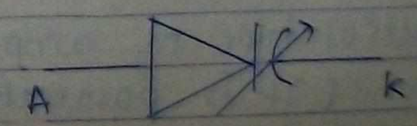
$$C_T \propto \frac{1}{\sqrt[3]{\text{R.B. VOLTAGE}}}$$

$$C_T \propto \frac{1}{\sqrt{V_{bi} + V_{RB}}}$$

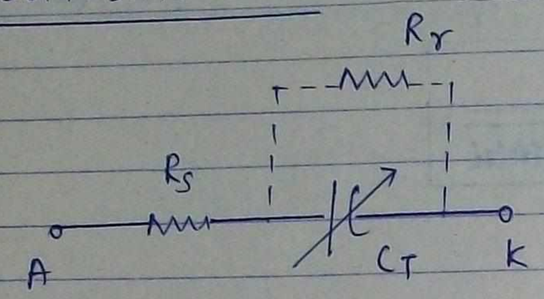
- Popularly used material is GaAs.
- Low noise device.
- CHARACTERSTIC CURVE -



- In a varactor diode, by varing R.B. voltage we get a small variation in C_T (few pf)
- In varactor diode by increasing R.B. voltage C_T is decrease.
- SYMBOL -



- EQUIVALENT CIRCUT -



R_s = ohmic resistance or contact resistance ($< 10\Omega$)
R_r = reverse resistance ($> 1M\Omega$)

- It is also called VARI-CAP DIODE (OR) VOLTA-CAP DIODE (OR) EPI-CAP DIODE.

- APPLICATIONS -

1. for direct generation of FM by using varactor diode modulator circuit.
2. for self balancing of a.c. bridges.
3. Balancing or Tuning of LC resonance circuit.
4. for fine tuning of receivers (R_x).
5. for electronic tuning of receivers
6. As an special type of amplifier as a PARA-amp. (It is parametric amplifier

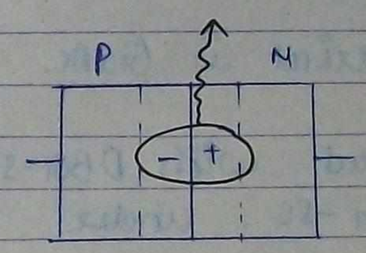
for GaAs $V_r = 1.3$ to $1.5V$

and it is a microwave power amplifier used with satellite communication.)

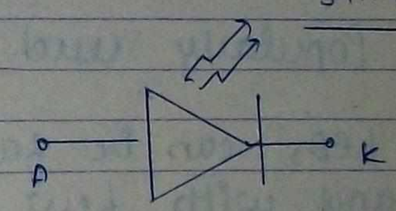
⇒ LIGHT EMITTING DIODE (LED) -

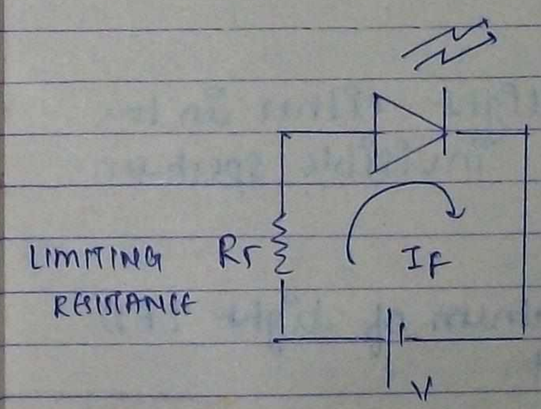
- PRINCIPLE -

ELECTRO-LUMINESENCE

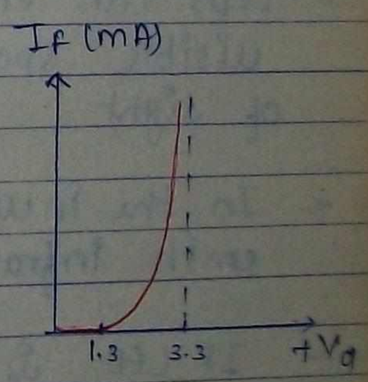


SYMBOL





CHARACTERSTIC -



- LED will emit the light when properly excited.

- PRINCIPLE -

ELECTRO-LUMINESENCE

- In LED light is emitted due to a large number of recombinations at the junction.

- The best electro-luminescence device is LED

- fabricated with DBG semiconductor.

- Popularly used material is GaAs.

- LEDs can be fabricated with DBG-SC. and with few IBG-SC. under controlled doping.

- LED's can emit the light either in the visible spectrum or invisible spectrum of light.

- In the invisible spectrum of light LED emits infrared light.

- IR LED is used as a remote controlled transmitter.

- In the visible spectrum of light LED can emit any one of the following colours: such as red, green, orange, yellow, white and Amber (light blue)

- The colour of light given by LED depends on
  1. The wavelength of radiated light.
  2. The frequency of radiated light

$$\boxed{\lambda = \frac{1.24}{E_G}} \ \mu m \quad , \quad \boxed{\lambda = \frac{c}{f}}$$

  3. The type of dopant.
  4. Concentration of dopant.

- LED fabricated with GaAs will emit infrared light.

- LED materials are:
  - GaAs → Infrared
  - GaAsP → orange, yellow
  - GaP → green.

- LED can emit single colour of light, but laser can emit multicolours of light.

- LED is always operated under forward bias.

- with 20 mA of forward current, LED gives out the maximum intensity of light.

- when LED is heated up (as temp increases) its efficiency decrease (it will emit dull colour light).

- when reverse biased, LED will work as an normal diode and therefore, it will not emit any light

- Cutting voltage, $V_r = 1.3V$ to $1.5V$ depending on dopants.

- Power dissipation $P_D = mW$ (also called internal power consumed.)

- Response time = μ sec.

- Operating life = 100000 + hrs

- LEDs are faster than LCDs. (because of smaller response time)

- When compare to LCD, the disadvantage of LED is higher power dissipation.

- APPLICATION -

1. As a remote control transmitter (major application)

2. As a display device.

3. In designing of OPTO-COUPLERS.

LIQUID CRYSTAL DISPLAY (LCD) -

- Power dissipation = μW.

- Response time = m sec.

- Operating life = 50,000 + hrs

- major application is as a display device.

- LED is made with liquid crystal material (popularly used material is PNEMATIC liquid)

- PRINCIPLE -
Dynamic scattering of light.

Que. A LED is fabricated with GaAs. Find its wavelength of radiated light at the room temperature.

Soln: $\lambda = \frac{1.24}{E_G}$ for GaAs $E_{G300} = 1.47$ eV

$\lambda = \frac{1.24}{1.47} = 0.843 \mu m$

Since $\lambda > 0.78\ \mu m$ LED fabricated with GaAs, will emit Infrared light.

Que. A Green colour LED emits light with a wavelength of 5490 A° units find the energy gap of the material used. in eV.

Sol^n: $1A^\circ = 10^{-10}\ m$

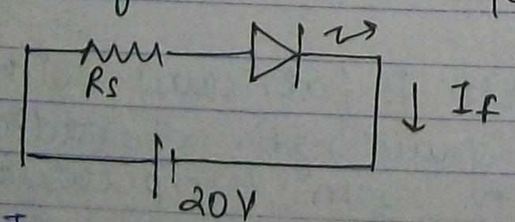
$$\lambda = 5490 \times 10^{-10}\ m$$
$$= 5490 \times 10^{-4}\ \mu m$$

$$\lambda = \frac{1.24}{E_G}\ \mu m$$

$$E_G = \frac{1.24}{5490 \times 10^{-4}}$$

$$E_G = 2.26\ eV$$

Que. for the LED circuit given below, find the value of limiting resistance required.



Sol^n: let $I_f = 20\ mA$
$V_d = 3.3\ V$

$$20 = I_f R_s + V_d$$

25/7/11

$$20 = 20 \times 10^{-3} \cdot R_s + 3.3V$$

$$R_s = 835\ \Omega$$

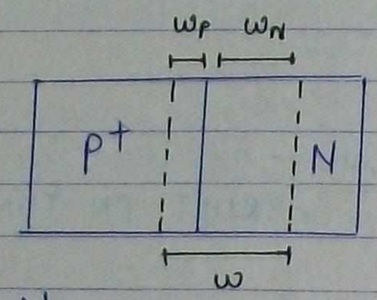
⇒ STEP GRADED DIODE –
(ABRUPT PN JUNCTION DIODE)

JUNCTION

NORMAL JUN.	ABRUPT JUN.
P | N	P | N
$N_A \equiv N_D$	$N_A \not\equiv N_D$
i.e equal doping for P and N region	Doping conc. are different b/w P and N region. Eg - P^+N or PN^+

- It has an abrupt junction.
- Eg P^+N diode or PN^+ diode
- faster than normal diode due to extra doping.
- depletion layer will be penetrating more into the lightly doped region and lesser into highly doped region.

① P^+N DIODE -



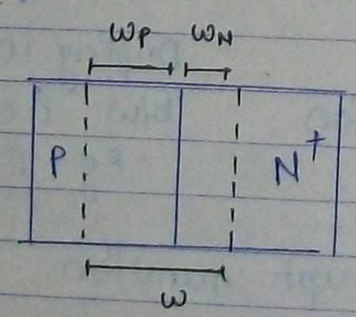
$N_A > N_D$

$W_N > W_P$.

since $W = W_N + W_P$ (W_P is negligible)

$$\boxed{W \simeq W_N}$$

② PN^+ DIODE -



$N_D > N_A$

$W_P > W_N$

$W = W_N + W_P$, $\boxed{W \simeq W_P}$

- In a step graded diode most of the depletion layer will be existing in the lightly doped region.

- Suppose if step graded diode is operating with reverse biased, then the equation for width of the depletion layer on the lightly doped region is given below:

① P^+N DIODE -

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) V_j}$$

Since N_A is large, $1/N_A$ is negligible and $W \simeq W_N$

$$\boxed{W_N = \sqrt{\frac{2\varepsilon}{q} \cdot \frac{V_j}{N_D}}} \text{ meters.}$$

The junction voltage V_j

$$\boxed{V_j = \frac{q N_D \cdot W_N^2}{2\varepsilon}} \text{ Volts}$$

② PN^+ DIODE -

Since N_D is large, $1/N_D$ is negligible and $W \simeq W_P$

$$\boxed{W_p = \sqrt{\frac{2\varepsilon}{q} \cdot \frac{V_j}{N_A}}}$$ meter

Junction voltage

$$\boxed{V_j = \frac{q N_A \cdot W_p^2}{2\varepsilon}}$$ volts.

- In the step graded diode the ratio of depletion layers on the p-side and N-side can be analysed by using charge equality equation, given by :

$$q A \cdot W_p \cdot N_A = q A W_N N_D$$

$$\boxed{N_A \cdot W_p = N_D \cdot W_N}$$

$$\frac{W_p}{W_N} = \frac{N_D}{N_A}$$

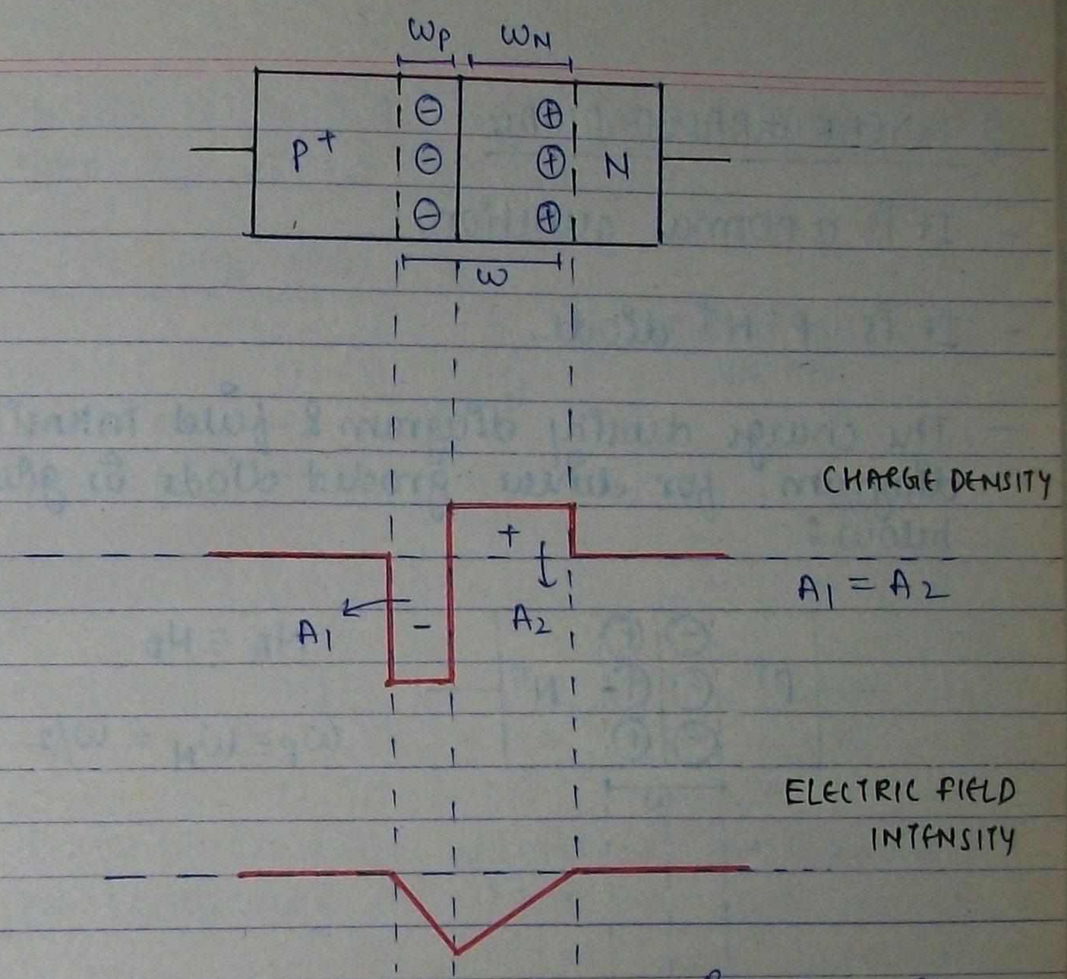
- The charge density diagram and field intensity diagram for the step graded diode is given below:

Consider P^+N diode.

$N_A > N_D$

$W_N > W_p$, $W = W_N + W_p$

$W \simeq W_N$

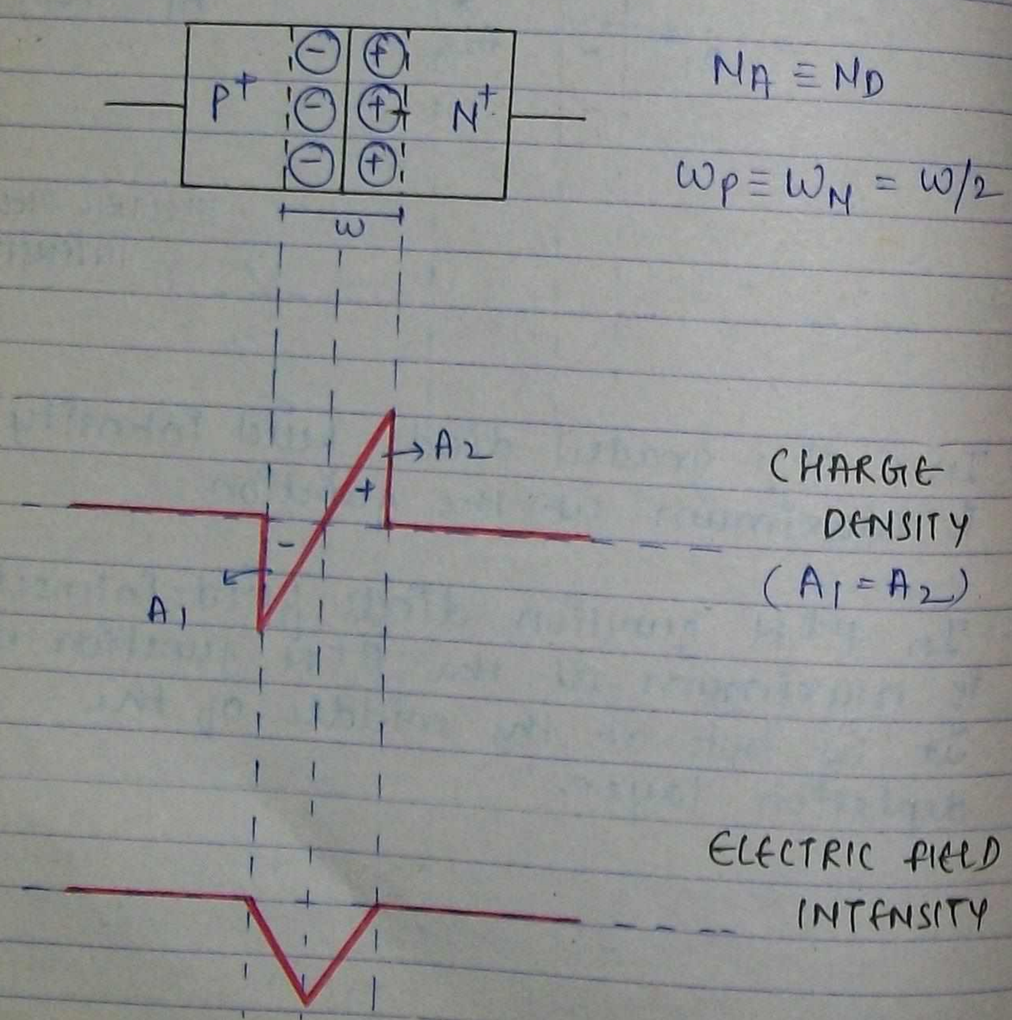


- In a step graded diode field intensity is maximum at the junction

- In P^+N junction diode field intensity is maximum at the P^+N junction but it is not at the middle of the depletion layer.

⇒ LINEAR GRADED DIODE -

- It is a normal junction.
- It is P^+N^+ diode.
- The charge density diagram & field intensity diagram for linear graded diode is given below:



$N_A \equiv N_D$

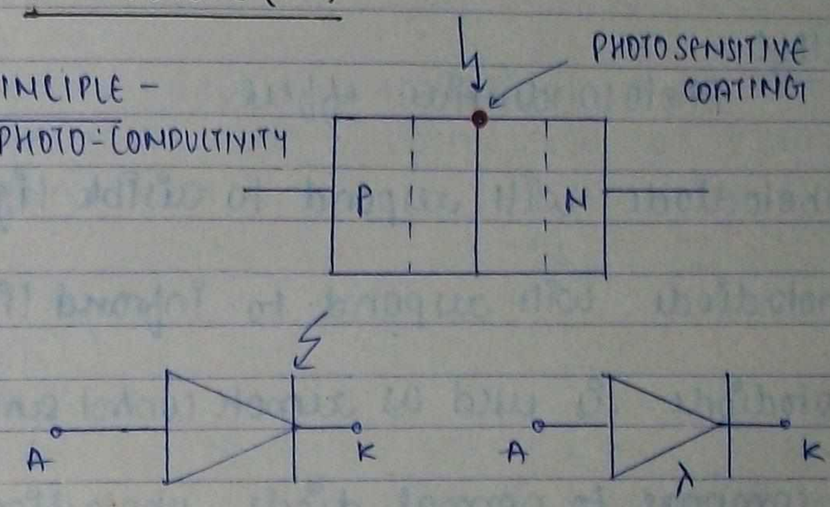
$W_P \equiv W_N = W/2$

- In linear graded diode field intensity is max at P^+N^+- junction.

⇒ PHOTODIODE (PD) -

PRINCIPLE -

PHOTO-CONDUCTIVITY



- A photosensitive device is the device will be responding to light.
- Basically a PN junction diode but having photosensitive junction
- Photodiode have normal junction i.e doping conc. are equal for P and N region.
- Photosensitive materials are CdS, Se, ZnS, PbS
- In a photodiode photosensitive coating is provided only at the junction.

- In a photodiode if light falls just away from the junction the device cannot be conducting.

- PRINCIPLE -
  Photoconductive effect.

- Ge photodiode will respond to visible light.

- Si photodiode will respond to infrared light.

- Si photodiode is used as remote control sensor.

- when compare to normal diode, photodiode has a larger depletion layer. and this is obtained by reducing the doping conc. of P and N regions.

- Photodiode has very high sensitivity. (& this is due to larger value of depletion layer)

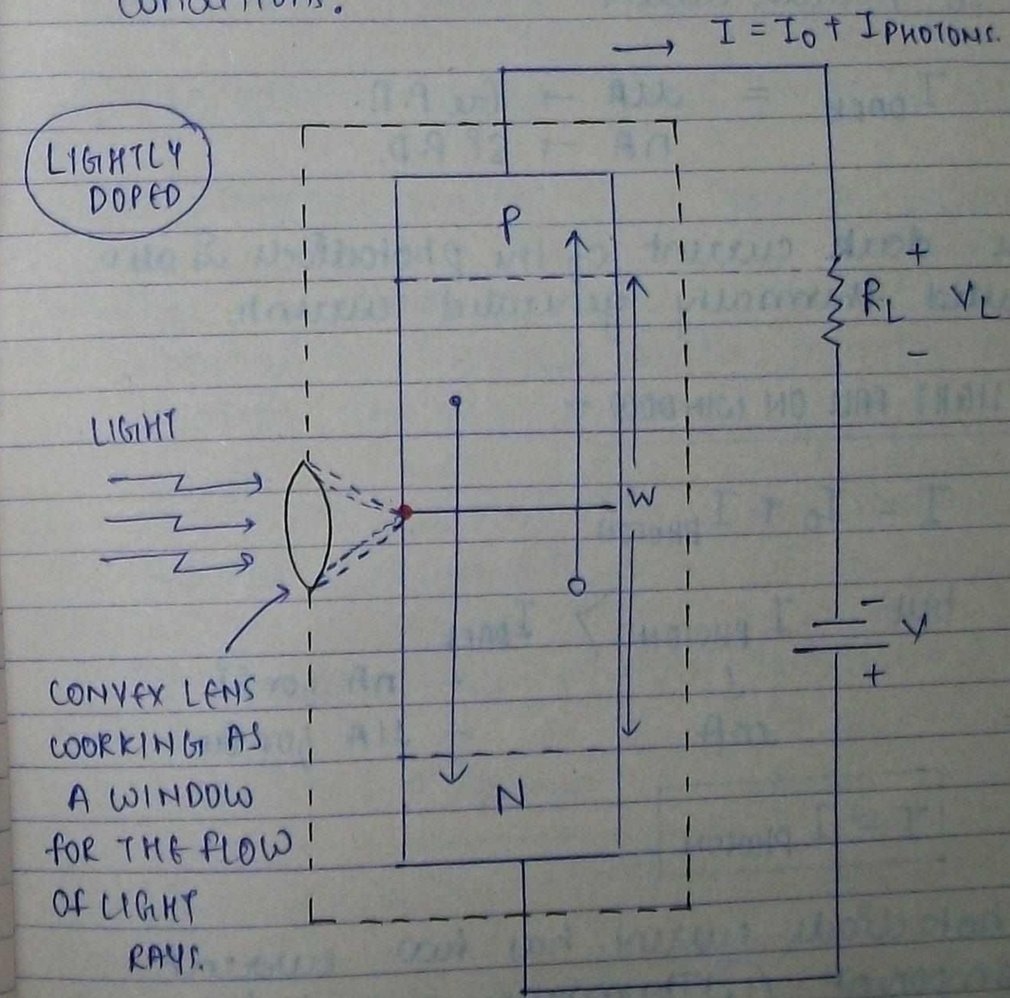
- Ability of the device to respond to the smallest value of I/P signal is called sensitivity.

- when compare to normal diode, photodiode is: 10 times faster,
  100 times higher sensitivity } advantages

- Low power handling (major disadvantage)

- Photodiode is generally operated under reverse biased.

- under special applications photodiode can be operated with open circuit or short circuit conditions.



UNDER DARKNESS –

$$I = I_0$$

↓

LEAKAGE CURRENT

(OR)

THERMALLY GENERATED CURRENT

$I_0 \Rightarrow$ Dark current

I_{DARK} = μA → Ge P.D.
nA → Si P.D.

- The dark current of the photodiode is also called thermally generated current.

WHEN LIGHT FALL ON WINDOW –

$$I = I_0 + I_{PHOTON}$$

but $I_{PHOTON} > I_{DARK}$

↓ mA

– nA for Si
– μA for Ge

$$\boxed{I \simeq I_{PHOTON}}$$

- Photodiode current has two current component (1.) Thermally generated current or I_{DARK} (2) photon current.

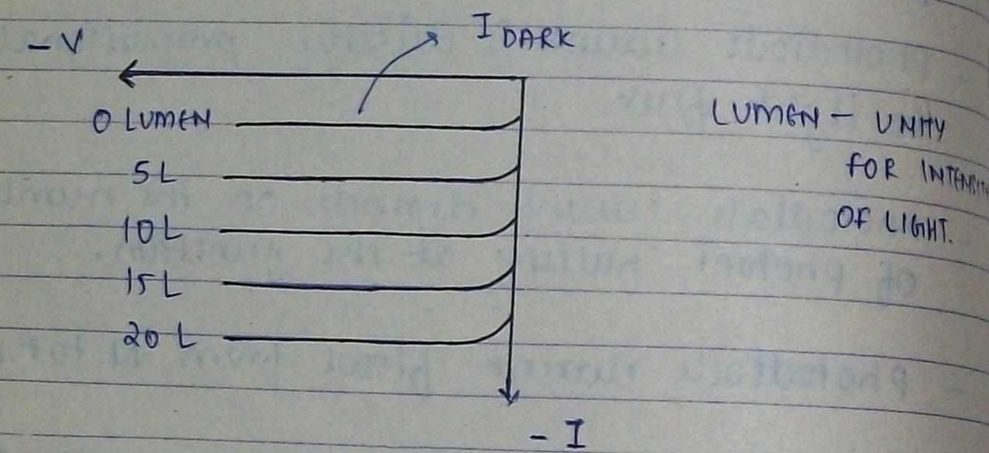
- Photodiode current is the sum of thermally generated current and photon current.
- Photodiode current is directly proportional to light flux.
- Photodiode current depends on the number of photons falling at the junction.
- Photodiode current flows from N to P region
- Photodiode current is a reverse current.
- The magnitude of reverse current in the photodiode increases with intensity of light falling at the junction.
- Photodiode current is a minority carrier current (since R.B.).
- The equation for photodiode current is

$$I = I_0 + I_{PHOTONS} \simeq I_{PHOTONS}$$

$$\boxed{I = I_S + I_0 \left[1 - e^{-V/nV_T} \right] \text{ Amp.}}$$

I_S = short circuit current of Photodiode

- Photodiode characteristics will be plotted in 3rd quadrant and is given below:



- Photodiode is basically a light operated switch.

- For a good photodiode the essential requirement is larger $\frac{I_{PHOTON}}{I_{DARK}}$ ratio.

	Ge PD	Si PD
$\frac{I_{PHOTON}}{I_{DARK}}$ =	$10^3:1$	$10^6:1$

- The disadvantage of Ge photodiode is small I_{PHOTON} / I_{DARK} ratio.

- Photodiode current is Diffusion current.

light → minority carrier.

- Photodiode is a minority carrier injector.

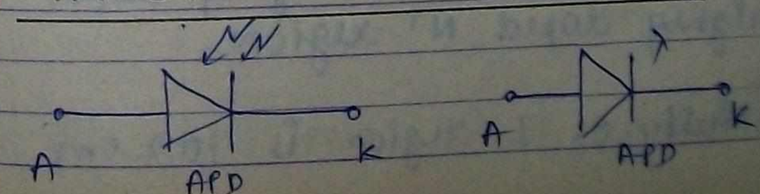
- APPLICATIONS -

1. As a remote control sensor (major appl^n)
2. In designing of optocouplers.
3. To read the audio track recorded on motion picture film.

NOTE - when photodiode is forward biased and light will focused at the junction it will work as a normal diode and the current is due to majority carrier.

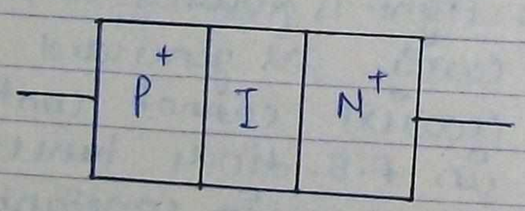
- when light is focused at the junction minority carrier are generated and this minority carrier cannot contribute the current in F.B. diode hence, the forward current will remain constant. Otherwise there will be no effect of light under forward current.

⇒ AVALANCHE PHOTODIODE (APD) -



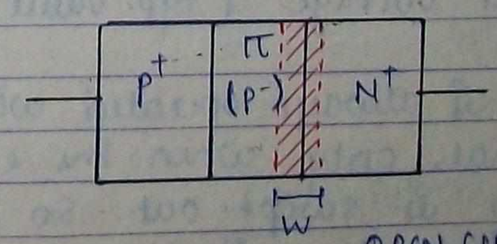
- Basically a photodiode along with avalanche effect.
- Response time is very small (75 ns typ. value)
- APD is faster than PD. because of smaller response time.
- fabricated only with Si.
- Always operated under reversed biased.
- Can be used as a receiver in fibre optics communication.

⇒ **PIN DIODE -**



- A microwave fast switch
- In PIN diode the intrinsic S.C is sandwitched in between highly doped P+ and highly doped N+ regions.
- The resistivity of I-region is 10Ω cm
- The smaller switching time of PIN diode is due to high resistivity offered by I-region.
- Popularly used material is GaAs.
- PIN diode is a three layer and two terminal device.
- In a practical PIN diode if I region is replaced by slightly doped P⁻ region (called π region) and the device is called PπN diode.
- In a practical pin diode if I region is replaced with slightly doped N⁻ region (called γ region), the device is called PγN diode.

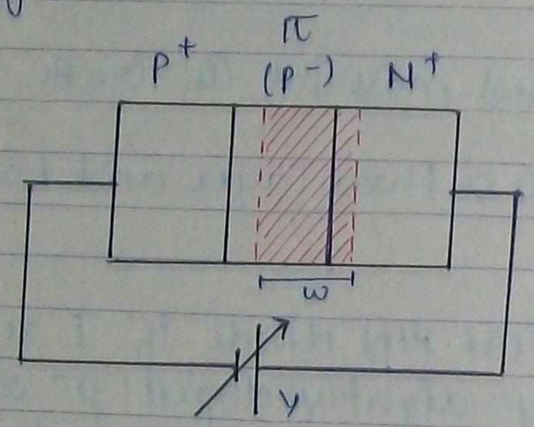
PπN DIODE -



OPEN CIRCUITED PπN DIODE

- PIN diode has a single junction.

- In open circuited PIIN diode, most of the depletion layer is existing only in the II region.



- PIN diode is always operated under reversed biased.

- By increasing R.B. voltage the entire II-region can be swept out.

- The minimum voltage required to swept out the entire II-region is called swept out voltage (typ. value -2V)

- PIN diode is always operated with an input signal, only when the entire II-region is swept out. So that there is no signal loss in the device.

- For I/P signal frequencies below 10 GHz

UJT, TD, GUN D } ONLY 3 -ve RESISTANCE S.C. DEVICE. (V∝1/I)

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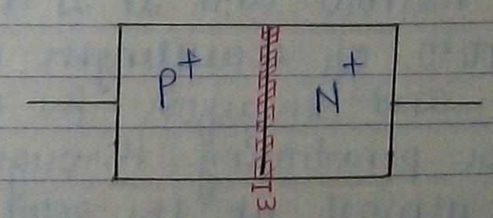
pin diode will be working as a normal diode.

- PIN diode can be used to handle large amount of microwave power, but it cannot generated the microwave power hence PIN diode is called passive microwave device. (diode)

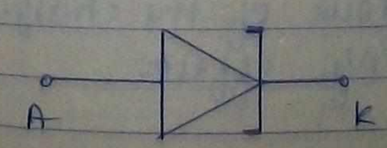
- PIN diode can be used as microwave detector, microwave mixer, microwave switches such as T-R switch (transmit-receive switch) and ATR (anti transmit receive) switch.

- As a duplexer (used in radar)

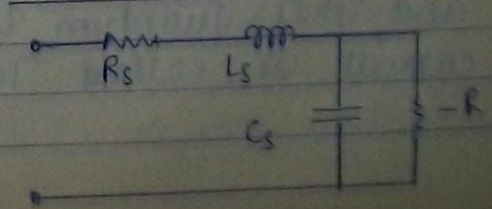
⇒ TUNNEL DIODE (TD) - (ESAKI DIODE).



SYMBOL -



EQUIVALENT CKT -



(*) most better heavily doped S.C. device. (exhibit metallic prop)

- Also called ESAKI diode.
- Basically P^+N^+ diode, with a normal junction.
- Doping conc. is $1:10^3$
- Narrow depletion layer (100 Å to 200 Å unit)
- exhibits the property of tunnelling effect.
- Popularly used material is GaAs.
- fastest switch.
- Switching time is in Picosecond (10^{-12} s)

(*) - Negative resistance (-R) device.

(*) - In tunnel diode the width of the depletion layer is very narrow and it is almost equal to 1/50th of wavelength of the visible light. and therefore the charge carriers will be penetrating through the depletion layer almost at the speed of light as if there is a tunnel in the device. and this quantum behaviour of the charge carriers is called Tunneling effect.

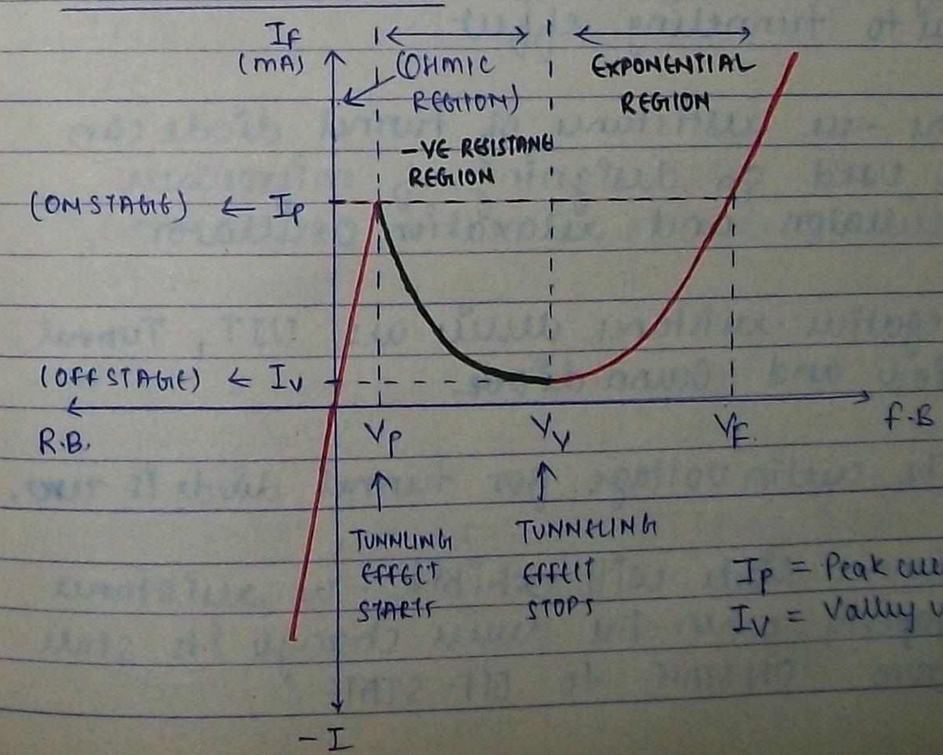
- ADVANTAGE -

1. Smaller in size, 2. easier to fabricate
3. economical, 4. negligible power dissipation
5. offers very high resistance to radiation

- DISADVANTAGE -

1. It is a two terminal device and therefore there is no proper dc isolation in b/w output and I/P sections.
2. Smaller voltage swing.

- VI CHARACTERSTICS -



- A reverse biased tunnel diode will be working as a linear device ie as a resistor.

- In the exponential region tunnel diode will be working as a normal diode.

- Tunnel diode is generally operated in Negative resistance region.

- In tunnel diode, -ve resistance means as forward voltage increases, the forward current decreases.

- Negative resistance of tunnel diode is due to tunneling effect.

- The -ve restistance of tunnel diode can be used in designing of microwave oscillators and relaxation oscillator.

- Negative resistance devices are UJT, Tunnel diode and Gunn diode.

- The cutin voltage for tunnel diode is zero.

- Tunnel diode will exhibit -ve resistance property when the device changes its state from ON STATE to OFF STATE.

- Tunnel diode exhibits -ve resistance property when the device:
  1. forward voltage changes from V_P to V_V.
  2. forward current changes from I_P to I_V.

- The operating point or Q-point of the tunnel diode is located in middle of the negative resistance region.

- for a good tunnel diode the essential requirement is large $\left(\frac{I_P}{I_V}\right)$ ratio.

	GaAs	Ge	Si
$\left(\frac{I_P}{I_V}\right) =$	15	7.5	2.5

- Tunnel diode can be fabricated either with GaAs or with Ge. and never with a Si material.

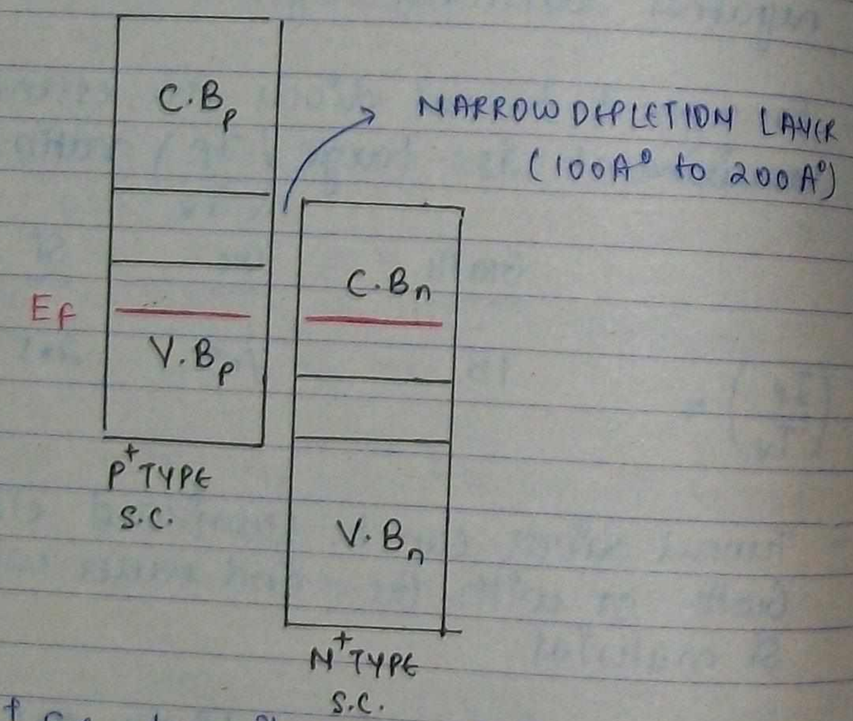
- High quality tunnel diodes are made with GaAs.

- Commercial tunnel diodes are made with Ge.

- Tunnel diode will exhibits multifeatured property or tripple valued property.

- Tripple properties in any value of forward current between I_V and I_P can be obtain with three different sets of forward voltages and due to this property tunnel diode more popular in pulse circuits & in industrial applications.

NOTE -

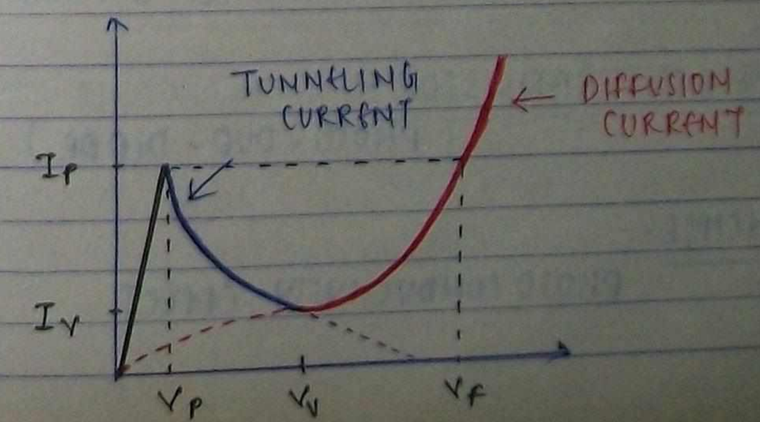


- In P$^+$ S.C fermi-level is in the valence band and in N$^+$ S.C. fermi level is in the conduction band, for the energy band diagram of the tunnel diode, the fermi level will maintain a straight line (level)

- when tunnel diode is properly forward bias ($\geq V_P$), the covalent bond will be broken in the valence band of P$^+$ S.C. and the electrons generated will be tunneling into the conduction band of N$^+$ S.C.. So that the electron conc. will become very large and mobility of the charge carrier (electron) decrease and therefore conductivity (or) forward current decrease.

- As forward voltage is gradually increasing from V_P to V_V the electron conc. will be increasing and mobility of the electrons decrease and therefore the forward current decrease and this property is called Negative Resistance and this is due to the tunneling effect.

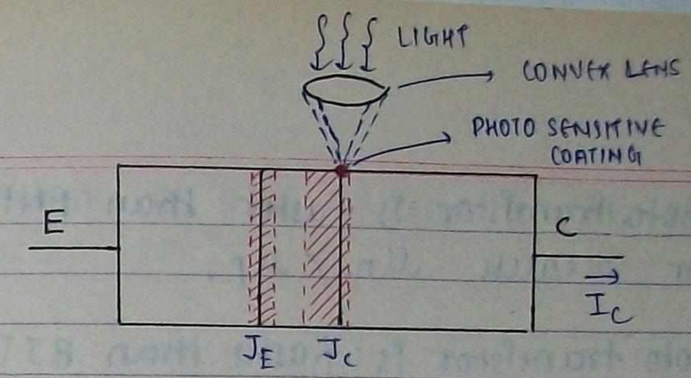
- The forward characteristic of tunnel diode can be plotted as:



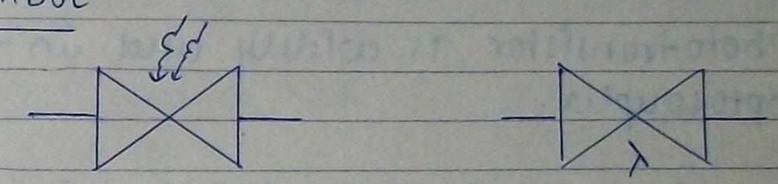
- Tunneling current is very high at peak point
- Tunneling current is very small at valley point
- Beyond the valley voltage, tunneling current reduces to zero.
- Diffusion current is very small at valley point.
- Beyond valley voltage, diffusion current exponentially increases with forward voltage.
- Diffusion current is ~~max.~~ o very high at peak current.
- Tunnel diode can be used in designing of negative resistance oscillators
  Ex- tunnel diode relaxation oscillators.
- Tunnel diode can be used as a PARA-amplifier

⇒ PHOTO-TRANSISTOR -
(PHOTO-DUO-DIODE)

- PRINCIPLE-
PHOTO CONDUCTIVITY EFFECT

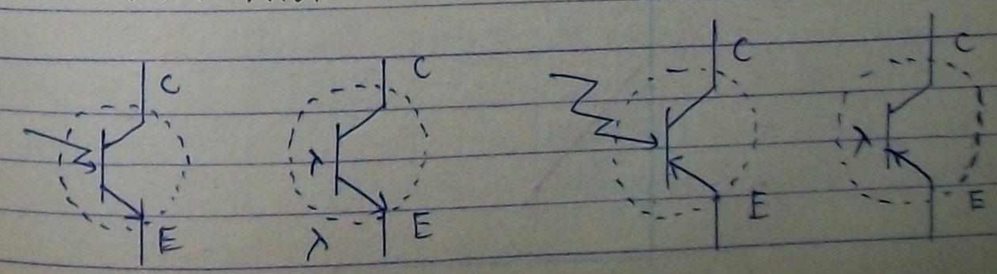


- SYMBOL -



- J_C is made photosensitive
- Phototransistor can be used as a light operated device
- Compare to normal diode, phototransistor is:
  1. 10 times faster } ADVANTAGE
  2. 100 times higher sensitivity
  3. Low power handling (DISADVANTAGE)

PHOTOTRANSISTOR
- NPN PHOTO. TRAN.
- PNP PHOTO. TRANS.



- NPN photo-transistor is faster than PNP photo transistor because $\mu_n > \mu_p$.

- FET photo transistor is faster than BJT photo-transistor.

- Photo transistor is widely used in the optocoupler.

⇒ **LIGHT DEPENDENT RESISTOR (LDR) -**

LIGHT ACTIVATED RESISTOR (LAR)

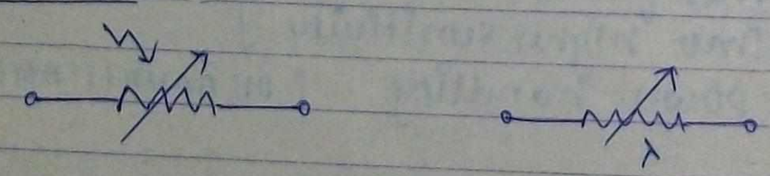
OR

PHOTO RESISTOR.

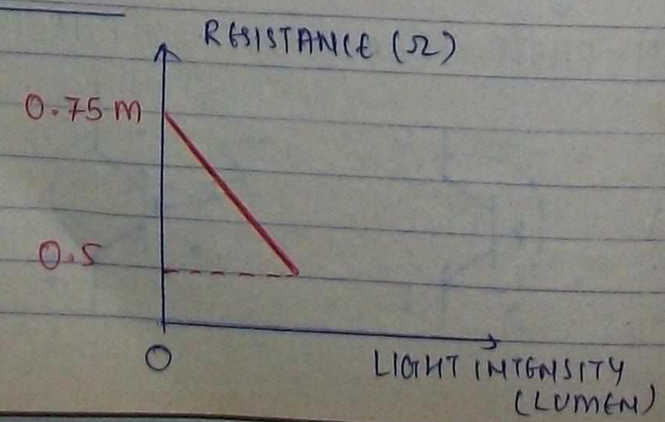
- **PRINCIPLE -**

PHOTORESISTIVE EFFECT

- **SYMBOL -**



- **LDR CHARACTERSTIS -**



- Resistance of LDR depends on the light falling on it.

- The resistance of LDR decreases with light.

- Range of resistance is from 0.75 MΩ to 0.5 Ω

- Dark resistance of LDR is 0.75 MΩ

- When LDR is highly illuminated, its resistance is 0.5 Ω

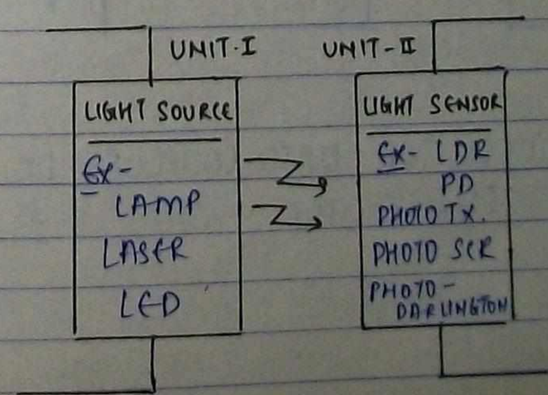
- Popularly used material is CdS, Se.

- LDR is an example of Passive component.

- LDR is used in opto-couplers.

⇒ **OPTO COUPLERS -**

(OPTO-ISOLATORS)



- They are optically coupled ~~up~~ but electrically isolated.

- Optocouplers are used in industrial applications where a very good dc isolation between than a transformer is required.

- Optocouplers are faster than conventional devices.
  - 10 times faster.
  - 100 times higher sensitivity.

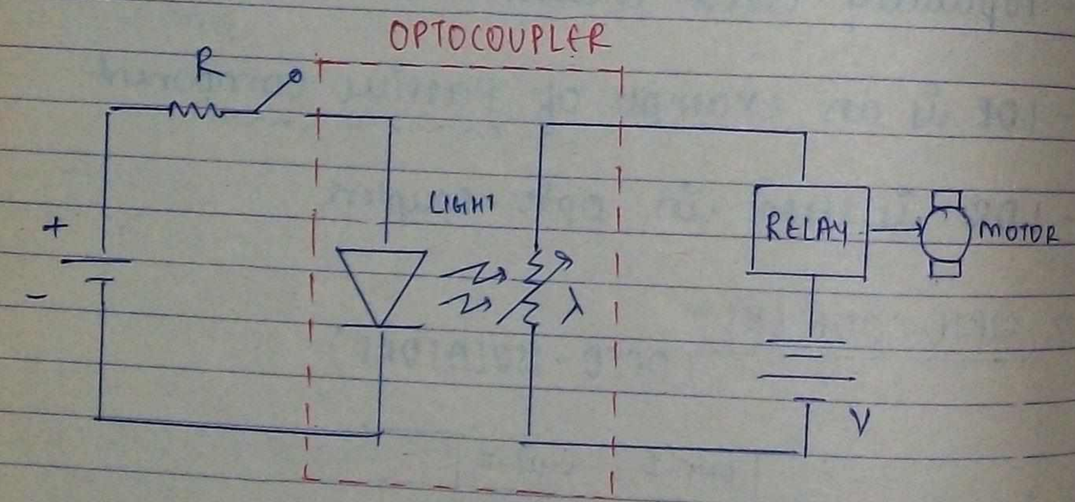


FIG: LED - PHOTORESISTOR OPTO COUPLER DRIVING THE MOTOR.

THYRISTORS

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- Basically a latch is having two stable state is ON state and OFF state.

- fabricated only with Si.

- Can handle large amount of power with negligble internal power consumption.

- Bistable device.

- Basically a multilayer S.C. device.

- Thyristors can be three layered, 4 layered and 5 layered solid state devices. (is made up of P and N-type material)

- When thyristor changes state from OFF to ON due to the applied current it is called CURRENT OPERATION.

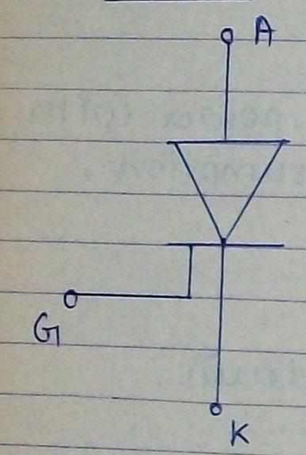
- If thyristor changes its state from OFF to ON due to the applied voltage it is called VOLTAGE OPERATION.

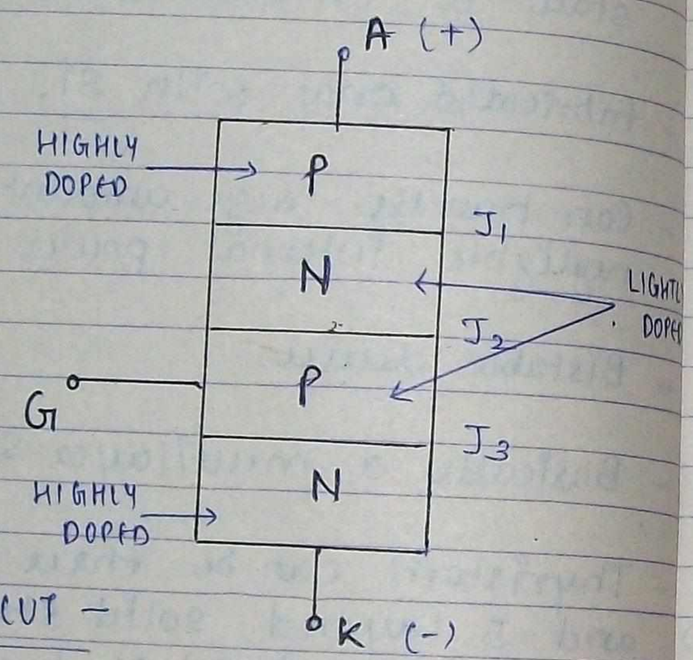
- Ge. thyristors are not pratical.

- Thyristor family members are:
  SCR, SCS, SVS, SBS, TRIAC, DIAC, PNPN DIODE, UJT

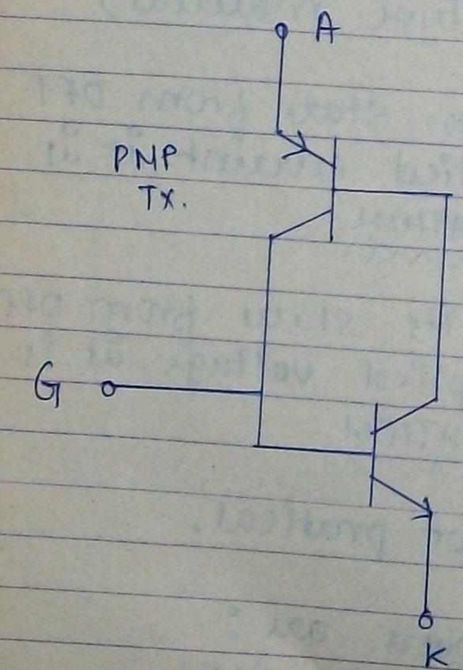
⇒ SILICON CONTROLLED RECTIFIER (SCR) -

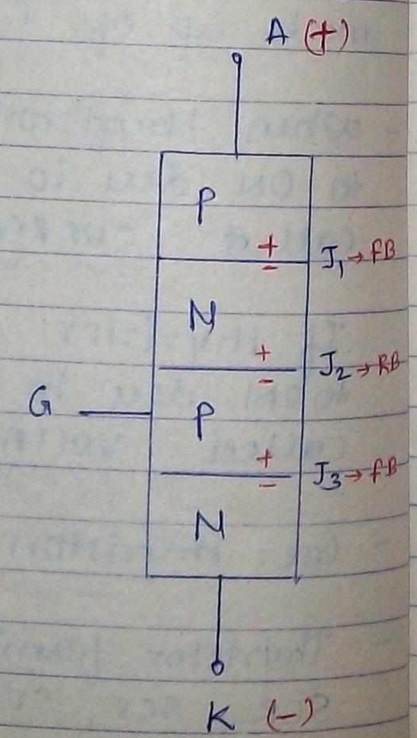
- SYMBOL -





- EQUIVALENT CIRCUT -



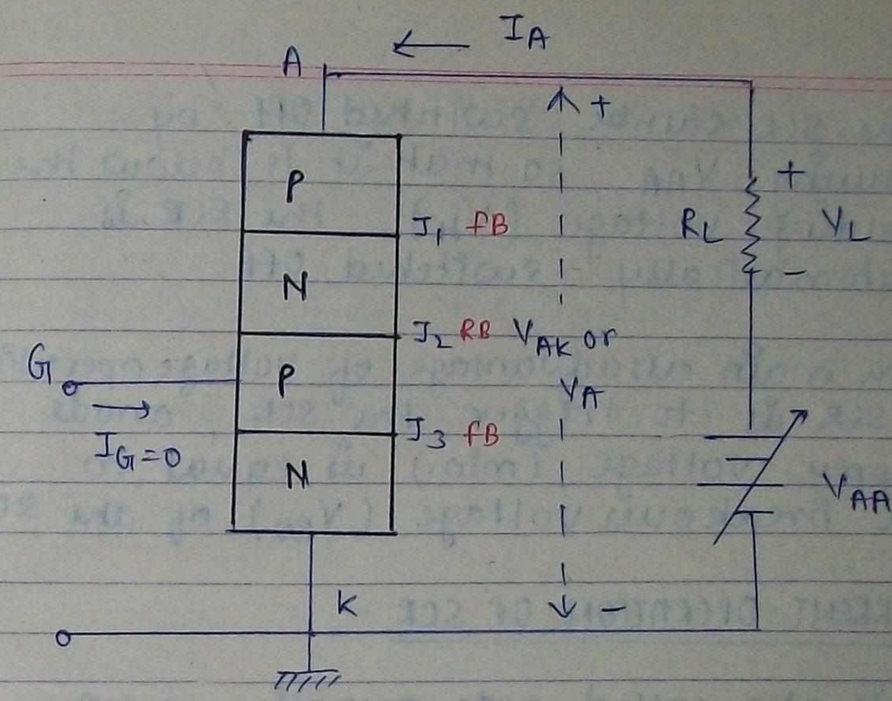


- Thyristor family member
- Three terminal device (anode, cathode, gate)
- four layer solid state device with three junctions.
- Power controlled device.
- Power switching device.
- unidirectional device (ie SCR can conduct only when anode is +ve with reference to the cathode)
- In SCR if anode is given -ve voltage, the SCR will not conduct.
- SCR can be voltage operated or current operated.
- The equivalent circuit of SCR is given by a transistor latch.
- The eq. circuit of SCR consist of one PNP transistor and one NPN tx. connected such that the collector of first tx. is given to base of second tx.

and collector of second tx. is given to the base of first tx.

- SCR is always operated under F.B.
- The breakover voltage of the SCR will be in the range of 50 V to 1800 V.
- SCR can be fabricated with MESA technology.
- SCR can be used as a fast switch.
- The switching time of SCR is nanosec (ns)
- when SCR is F.B. by a small voltage (less than breakover voltage (V_{BO})) and if gate is open circuited, J_1 and J_3 are F.B and J_2 is R.B. and the internal resistance of the SCR is greater than 1 MΩ and the anode current is zero, the SCR is now in OFF state. (non conducting state), or (forward blocking state).

⇒ VOLTAGE OPERATION OF SCR –



- for voltage operation of SCR the gate current must be kept zero.
- If anode supply voltage (V_{AA}) is less than V_{BO}, J_1 and J_3 are F.B. and J_2 is R.B. and the anode current is zero, the SCR is in OFF state i.e forward blocking state.
- If anode supply voltage (V_{AA}) is gradually increased, the reversed biased junction J_2 is become more & more reversed biased, when anode supply voltage equal V_{BO}, the reversed biased jun. J_2 will breakdown and a large anode current flows. The SCR is now in ON state.

- The SCR can be switched off by reducing V_{AA}, so that it is below the holding voltage (V_H), the SCR is automatically switched off.

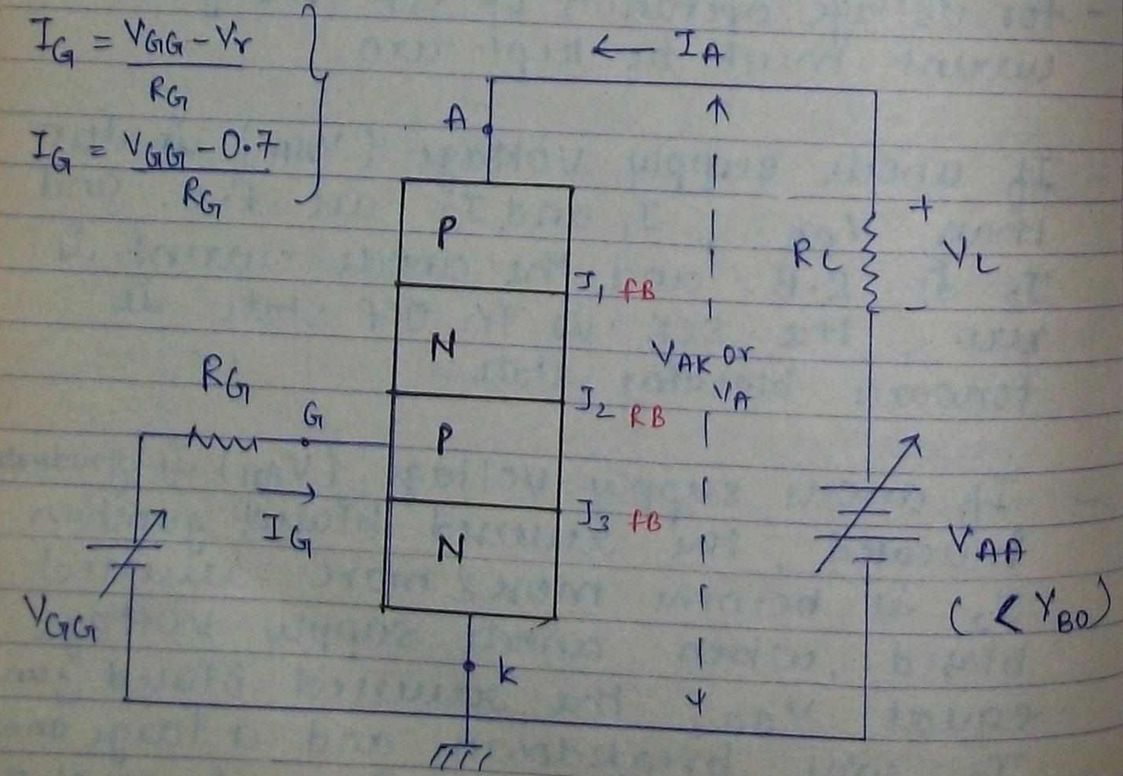
- The main disadvantage of voltage operation of SCR is to trigger the SCR, anode supply voltage (min.) is equal to the breakover voltage (V_{BO}) of the SCR

⇒ CURRENT OPERATION OF SCR -

- It is also called gate operation of SCR.

$$I_G = \frac{V_{GG} - V_r}{R_G}$$

$$I_G = \frac{V_{GG} - 0.7}{R_G}$$



① If $V_{AA} < V_{BO}$ & LET $I_G = 0$:

- Now SCR is in OFF state :

- J_1, J_3 are F.B and J_2 is R.B.

- Internal resistance of SCR > 1 MΩ

- $I_A = 0$

- $V_L = 0$ ($V_L = -I_A \cdot R_L$)

- Voltage drop across the SCR is V_{AK} or V_A is very large,

$$V_{AK} \simeq V_{AA}.$$

- P_D or internal power consumption is zero (since $I_A = 0$)

- The function of the gate is to trigger the SCR by sending a proper gate current.

- In SCR gate is made up of P-type S.C.

- gate to cathode of the SCR is always forward biased.

SCR max power handled = 50 Mwatt.

② IF $V_{AA} < V_{BO}$ & LET $I_G \neq 0$ (VERY SMALL) $\simeq 1mA$ -

- when SCR is in the ON state :

- J_1, J_2 and J_3 are f.B.

- Internal resistance of SCR is very small 0.1 Ω to 1 Ω.

- I_A is very large.

- Load voltage V_L is very large.
  $|V_L| \simeq |V_{AA}|$

- Voltage drop across the SCR (i.e V_{AK}) suddenly decrease to below 1V.

- Internal power consumed by SCR is P_D = very small $\simeq$ 1 W.

(*) SCR is not a Negative resistance device.

(*) when SCR is triggered at time t=0, the anode current instantaneously increases to a very larger value and at the same time the voltage drop across the SCR instantly falls below 1 V.

- The function of the gate is to trigger the SCR and once SCR is triggered and fired, the gate will be loosing its control on the SCR. and also on the anode current (i.e any variation in the gate current now, will not have any affect on the SCR and also on the anode current.)

- If SCR is triggered with a gate current of 1mA so that SCR is fired and the anode current is 10 Amp. If gate current is doubled then anode current of the SCR is 10 Amp (same).

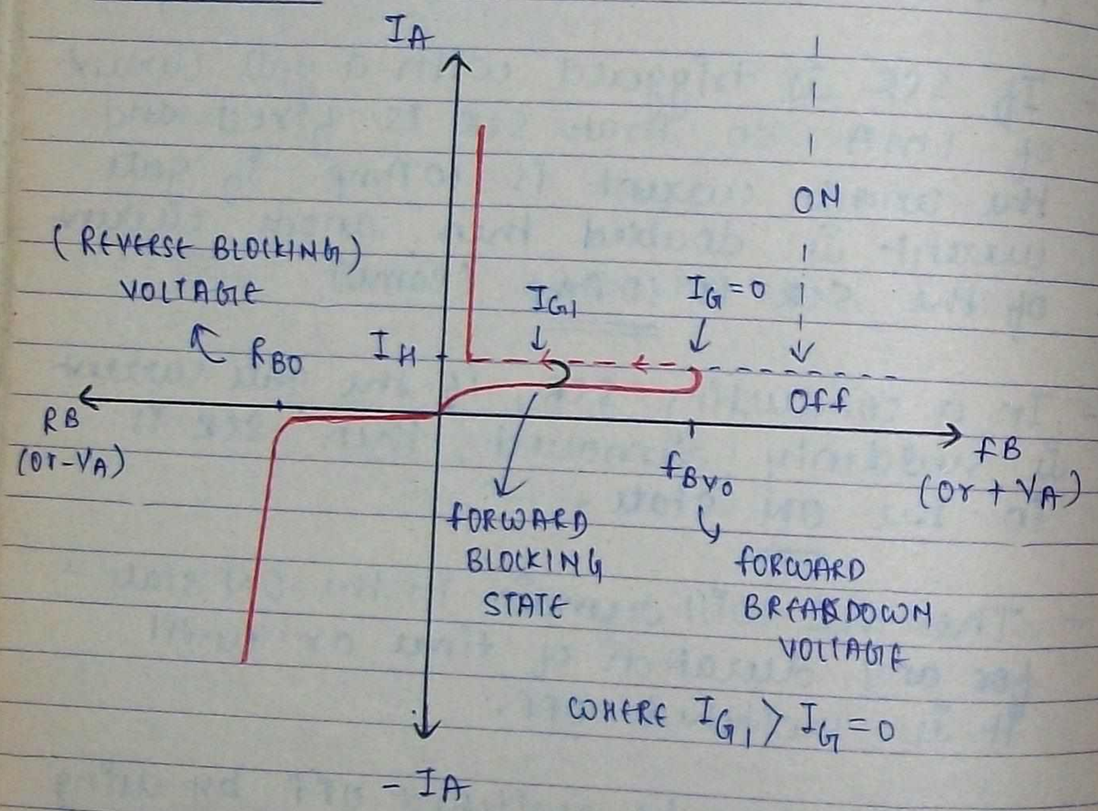
- In a conducting SCR, if the gate current is suddenly removed, then SCR is in the ON state.

- The SCR will remain in the ON state for any duration of time or until it is switched off.

- The SCR can be switched off by using any one of the following three methods:
  1. discontinue the power supply.
  2. make anode - ve wrt cathode.
  3. reduce anode supply voltage (V_{AA}) so that the anode current fall below the holding current (I_H). The SCR is switched off.

- Once SCR is OFF, the gate terminal will be regaining its control on the device. (i.e. if gate current is now applied the SCR can be triggered & fired.)

- THE V-I CHARACTERSTIC OF SCR FOR CURRENT OPERATION -



FIRING VOLTAGE OF SCR $\propto \frac{1}{I_G}$

- Current operation of SCR is more popular than voltage operation of SCR because we can fire the SCR with smaller anode voltage by applying larger gate currents.

- SPECIFICATIONS OF SCR -

1. SCR can handle max power as large as 50 Mwatt.
2. Break down voltages $V_{BO} \rightarrow$ 50 Vs to 1800 V.
3. SCR can handle anode current upto 2000 A.

(*) HOLDING CURRENT (I_H) -

It is the minimum anode current required to keep the SCR in the ON state.

- Holding current is sensitive to temp.
- Holding current decreases with increase in temp.
- In an SCR if anode current is greater than holding current SCR is in
  $I_A > I_H$ (ON STATE)
- In an SCR if $I_A < I_H$, SCR is in (OFF STATE)

⇒ **LATCHING CURRENT (I_{LATCH}) –**

- It is the minimum gate current required to trigger the SCR.
- Typical value of I_{LATCH} = 1 mA.
- In an SCR always $I_H < I_{LATCH}$.

⇒ **TURN ON TIME –**

- It is the time required to switch the SCR from Off state to ON state.
- Turn ON time increases with temp.
- Turn ON time decreases with increase of trigger voltage (V_{GG}).
- Turn ON time increases with increase in anode current.

⇒ **TURN OFF TIME –**

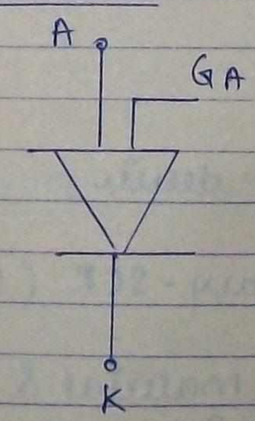
- It is the time taken to turn off the device.
- Turn off time increases with temp.
- Turn off time increases with increase in anode current.

NOTE – SCR can be used in polyphase rectifiers.

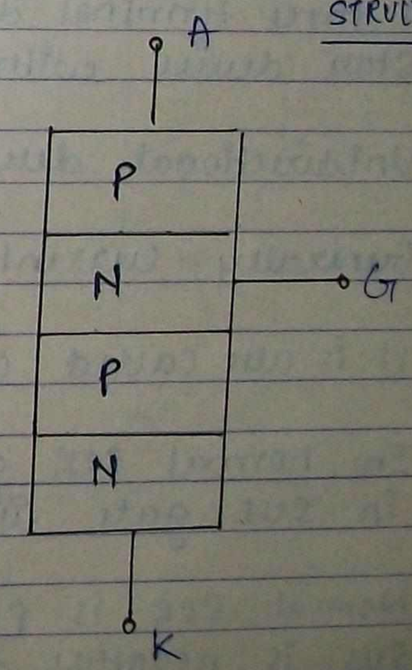
- SCR can be used for speed control of DC motors.
- The tube version of SCR is THYRATRON.
- Thyraton is gas triode.

⇒ **SILICON UNILATERAL SWITCH (SUS) –**

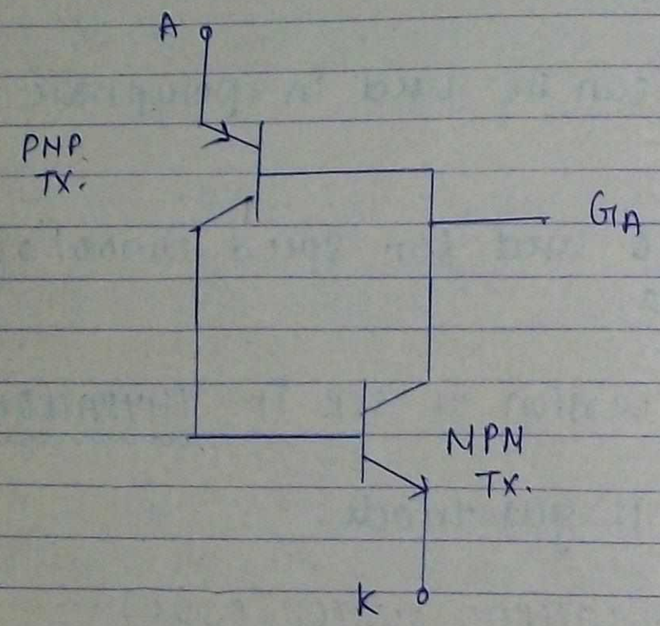
- SYMBOL –



STRUCTURE



- EQUIVALENT CIRCUT -

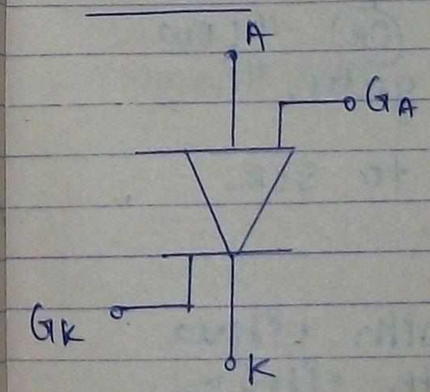


- A three terminal device, four layer solid state device with three junctions.
- Unidirectional device.
- Generally current operated device.
- It is also called complementary-SCR (CSCR)
- In normal SCR gate is P-material & in SUS gate is N-material.
- Normal SCR is positive triggered, while SUS is negative triggered.

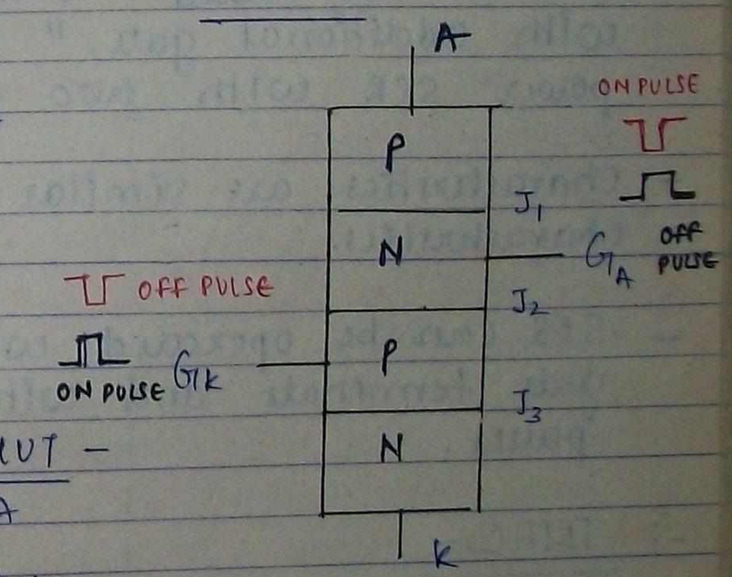
- Characteristics are similar to SCR.
- SUS can be used as an Relaxsation oscillator.
- SUS can be used as PUT (Programmable unijunction transistor).

⇒ SILICON CONTROLLED SWITCH (SCS) -

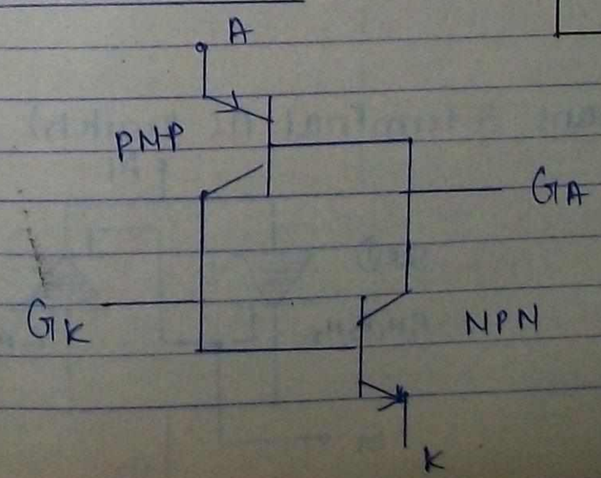
- SYMBOL -



STRUCTURE -



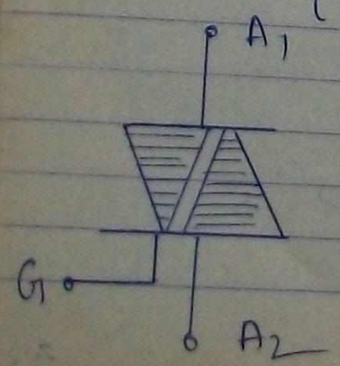
- EQUIVALENT CIRCUT -

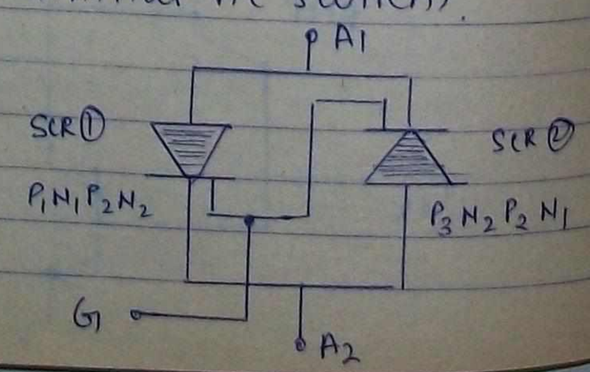


- four terminal device have Anode, cathode, anode gate & cathode gate.
- unidirectional device.
- current operation is more popular.
- four layer solid state device with three junctions.
- SCS is also called "Low power SCR with additional gate." (OR) "Low power SCR with two gates."
- Characteristics are similar to SCR characteristics.
- SCS can be operated with either gate terminals and with either pulses.

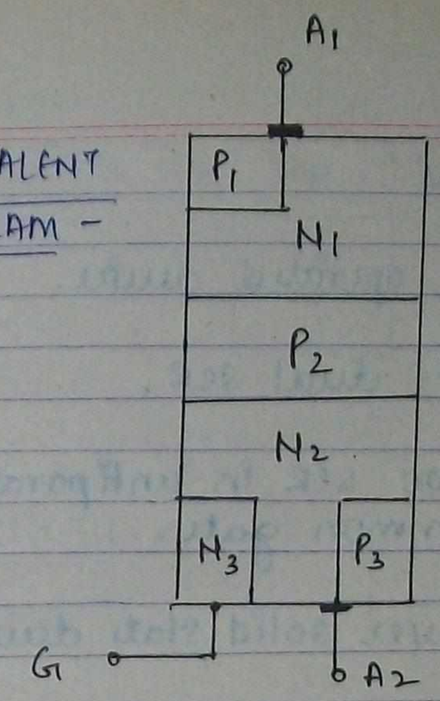
⇒ TRIAC -

(means 3 terminal AC switch)

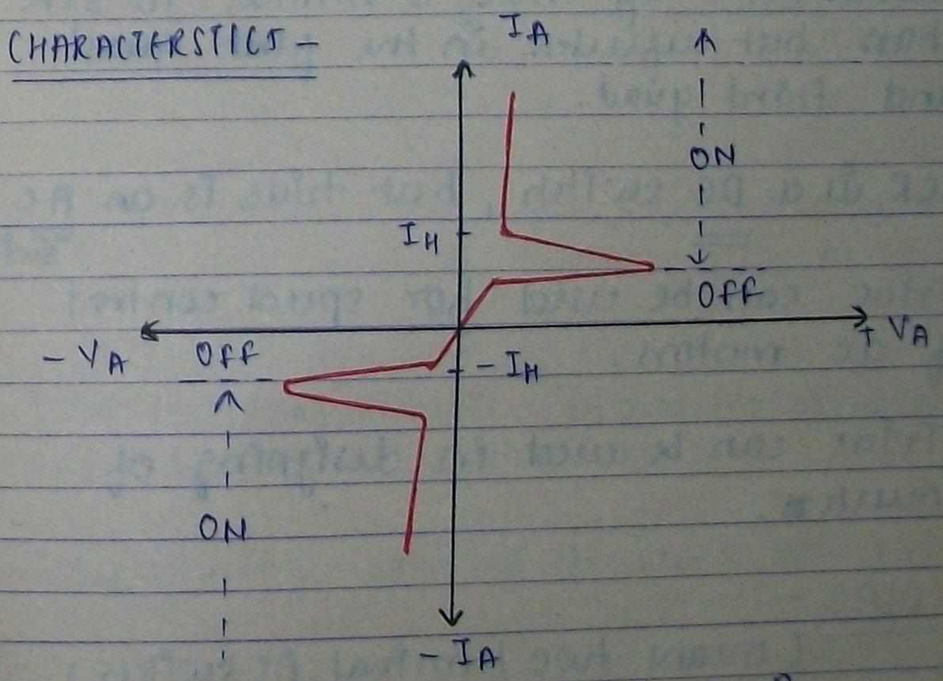




- EQUIVALENT DIAGRAM -



- CHARACTERSTICS -



- Triac is three terminal device (anode 1, anode 2 and gate).

- Bidirectional device.

- Generally current operated device.

- Triac is also called dual SCR.

- Triac consist of two SCR in antiparallel and with a common gate.

- Triac is a five layer solid state device.

- Characteristic of triac is similar to SCR char. but reflected in the first quad and third quad.

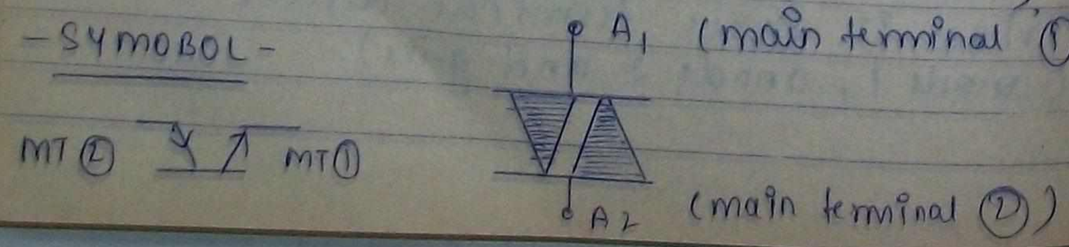
- SCR is a DC switch, but triac is an AC switch.

- Triac can be used for speed control of ac motors.

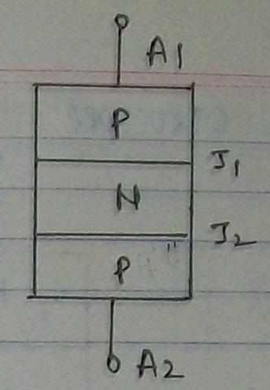
- Triac can be used in designing of Inverters.

⇒ DIAC –
(means two terminal AC switch)

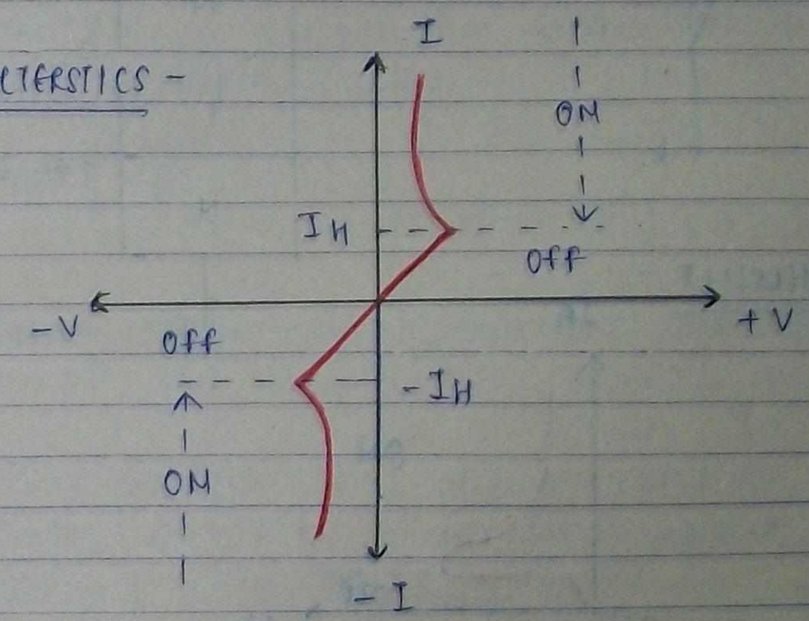
- SYMOBOL -



STRUCTURE –



CHARACTERSTICS –



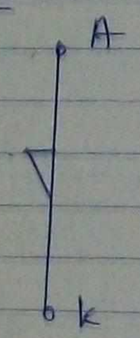
- Two terminal device, bidirectional device, three layer solid state device.

- Only voltage operated device. (since no gates are present)

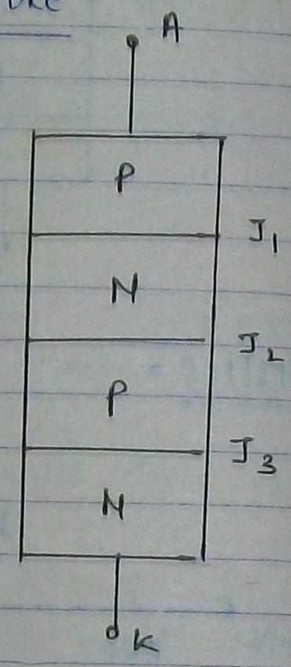
- DIAC can be used to trigger the SCR.

⇒ PNPN DIODE -

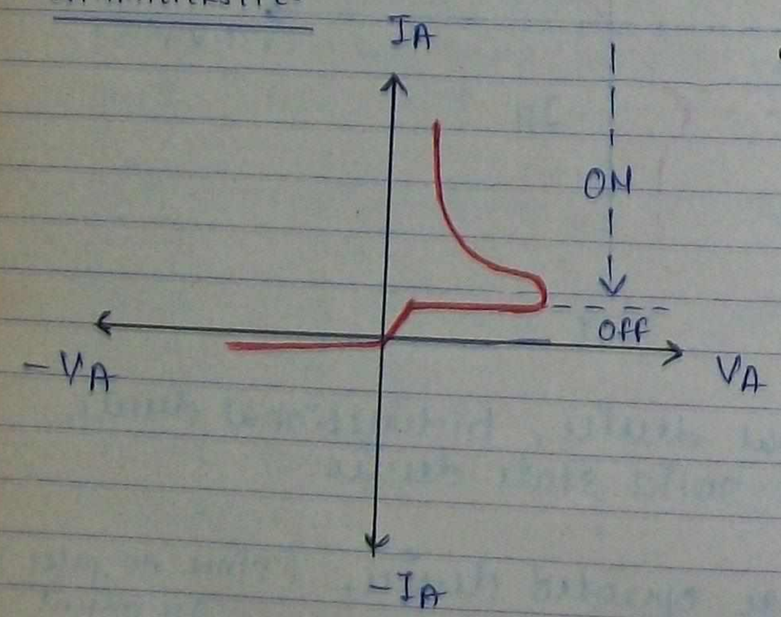
- SYMBOL -



STRUCTURE -



- CHARACTERSTICS -



- Popularly known as schokley diode
- Also called four layer diode
- unidirectional device.

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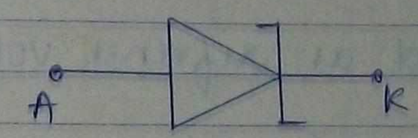
⇒ ZENER DIODE (Z_D) -

- SYMBOL -



- Basically a PN junction with little increase in the doping levels.
- Doping conc. $1:10^5$
  or $1:(10^5 \text{ to } 10^6)$
- Zener diode has a normal junction or abrupt junction.
- ⊛ when design with abrupt junction, zener diode exhibits, tunneling effect under reversed biased operation.
- ⊛ Zener diode operates on the principle of TUNNELING EFFECT or TUNNELING of CHARGE CARRIES across the junction.
- fabricated only with silicon.
- Also called breakdown diode.
- Popularly known as Constant voltage device.

- Major application is as a VOLTAGE REGULATOR circuit.

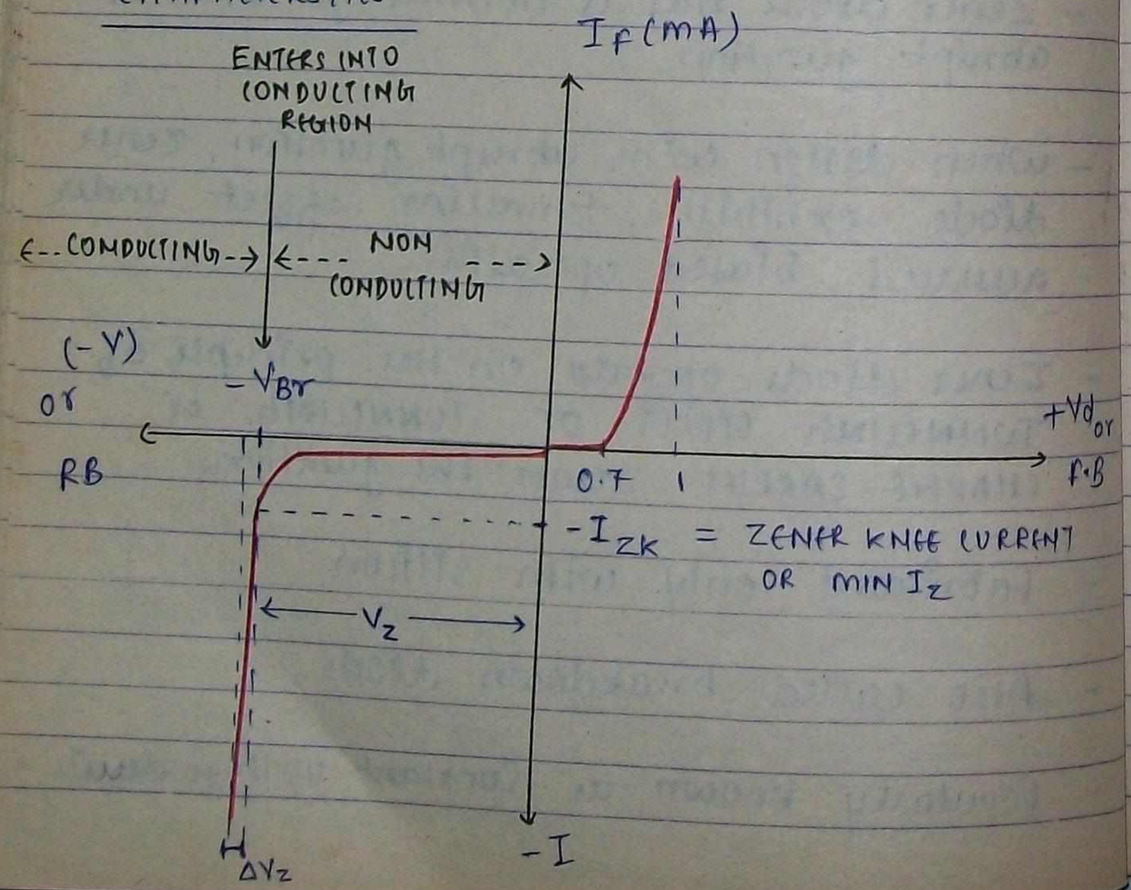
- Can be used as refrence voltage device.

- Always operated under reversed biased.

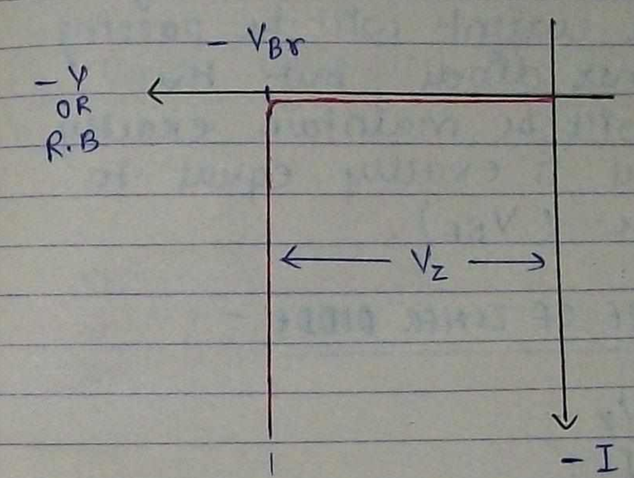
- When F.B. zener diode will be working as a normal diode.

- Cutin voltage for zener diode is 0.6 V or 0.7 V

- CHARACTERSTICS -



- VI CHARACTERSTIC OF IDEAL ZENER DIODE -



- In zener diode is reversed biased below the breakdown voltage, the current is practically zero and zener diode is non conducting. (at present it is working as a normal diode).

- When reverse voltage equals breakdown voltage, the current to the zener diode suddenly increases to I_{ZK} and this is due to breakdown phenomenon.

- When reverse voltages are greater than breakdown voltage, more and more current will be passing to the zener diode but the voltage drop across the device will be maintain almost a constant and it is around the breakdown voltage. (Hence ZD is called constant voltage device)

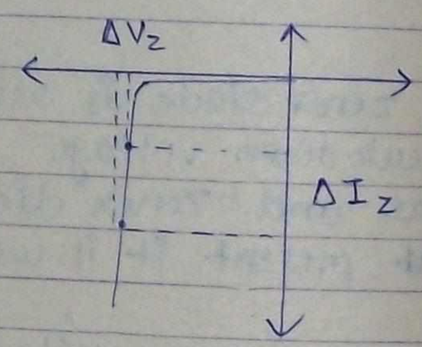
- In ideal zener diode, when reverse voltage are greater than breakdown voltage more and more current will be passing through the zener diode, but the voltage drop will be maintain exactly a constant and is exactly equal to breakdown voltage (V_{BR}).

- DYNAMIC RESISTANCE OF ZENER DIODE -

$$R_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

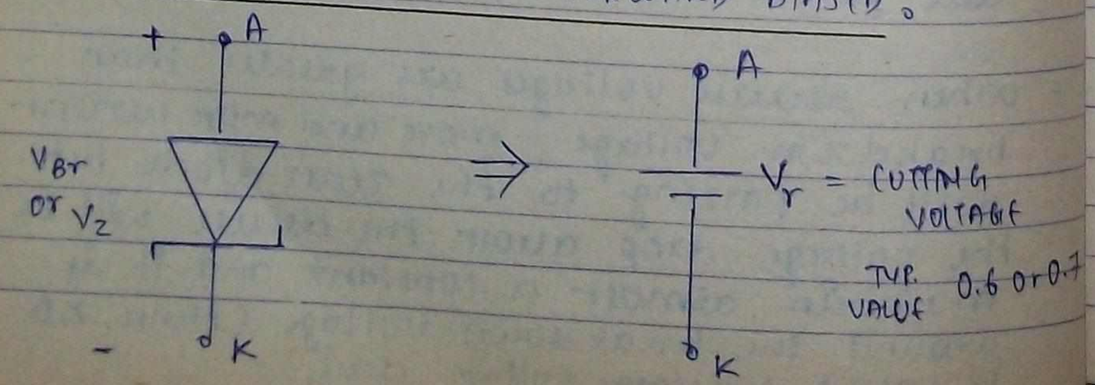
- for ideal zener diode dynamic resistance is zero.

$R_Z = 0 \quad (\Delta V_Z = 0)$



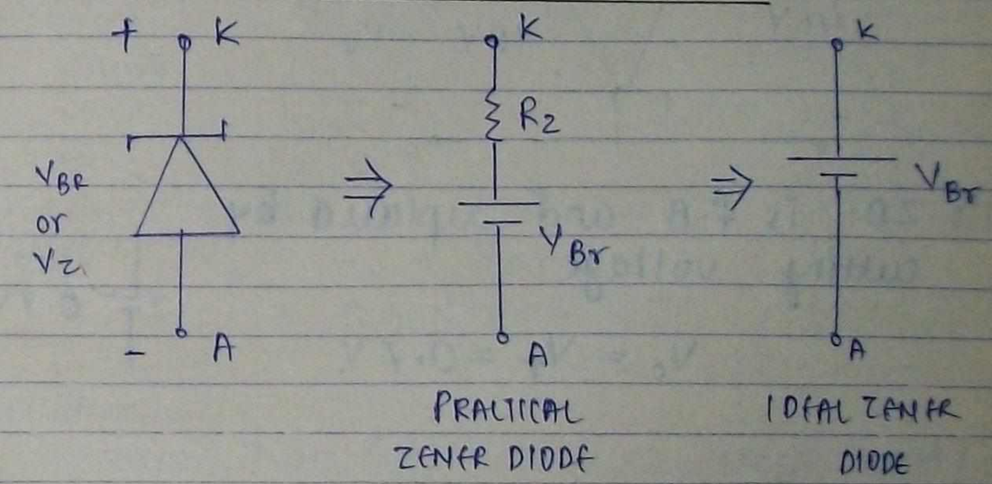
- EQUIVALENT CIRCUT OF ZENER DIODE -

(1) WHEN ZENER DIODE IS FORWARD BIASED:



- A forward biased zener diode can be replaced by its cuttin voltage.

(2) WHEN ZENER DIODE IS REVERSE BIASED:



- NOTE -

Zener diode are commercially available with V_{Br} in the range of 2.5V to 300V.

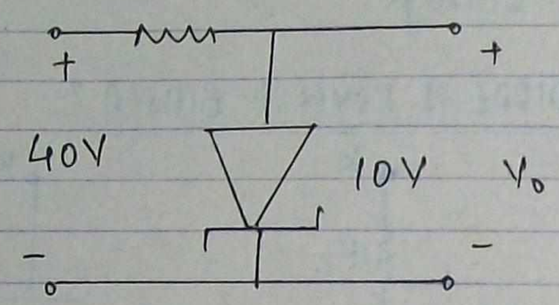
- Zener diode when operated as a voltage regulator circuit, will be working on the principle of TUNNELING EFFECT.

- Zener diode is specified in terms of V_{Br} (breakdown voltage) and P_{Zmax} (maximum zener power dissipation).

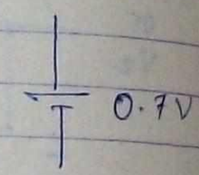
Ex - a zener diode has 10 V, 400 mV
(V_{Br}, P_{Zmax})

Que. find output voltage for the circuit given:

(1)

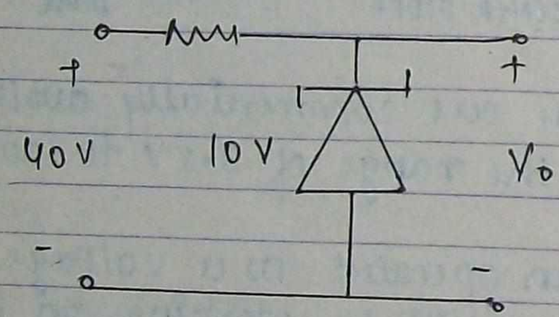


Soln: ZD is f.B and replaced by cutting voltage

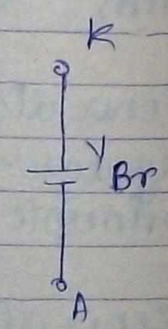


$V_o = V_r = 0.7V$

(2)

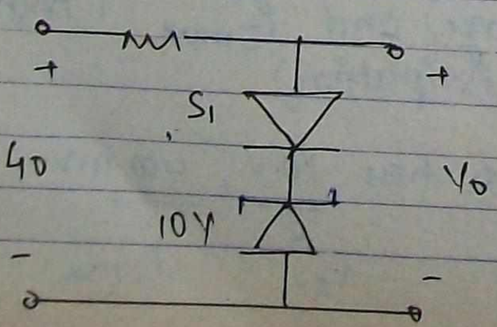


Soln: ZD is RB and replaced by its Breakdown voltage

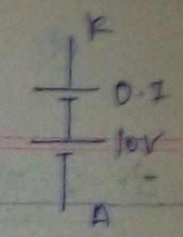


$V_o = V_{Br} = 10V$

(3)

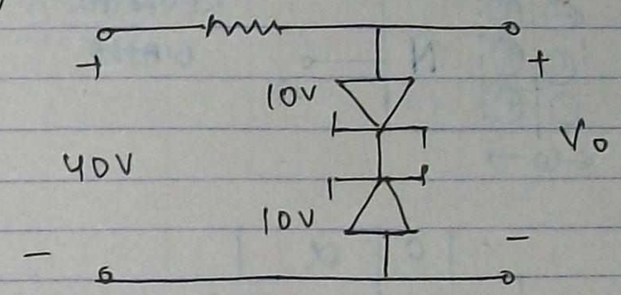


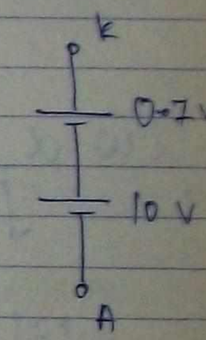
V_{Br} V_r



Soln: $V_o = 10V + 0.7 = 10.7V$

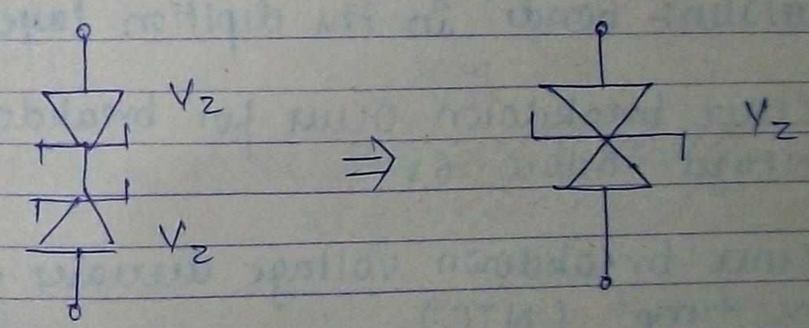
(4)



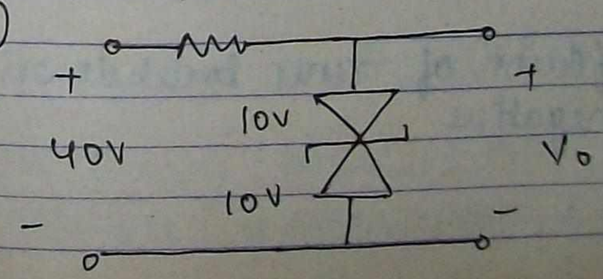


Soln: $V_o = V_r + V_{Br}$
$= 0.7 + 10 = 10.7V$

(*) NOTE -
when two identical zener diode are connected back to back, they can be replaced as



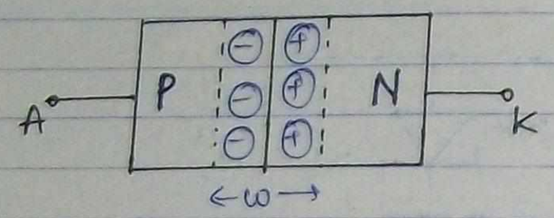
(5)



Ans 10.7

⊛ for zener to occur $V_{BR} < 6V$

⇒ ZENER BREAKDOWN PHENOMENON –



REVERSED BIASED

$\downarrow W \propto \frac{1}{\sqrt{\text{DOPING}\uparrow}}$, $\uparrow |\mathcal{E}| \propto \frac{1}{W\downarrow}$

$|\mathcal{E}| = 2\times10^{7}\ V/m.$

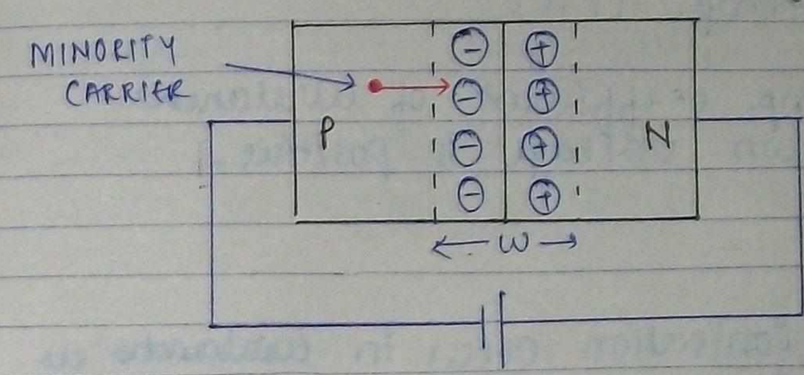
- It is due to larger electric field intensity.
- It is due to TEARING OFF or RUPTURING OFF covalent bonds in the depletion layer.
- Zener breakdown occur for breakdown voltages below 6V.

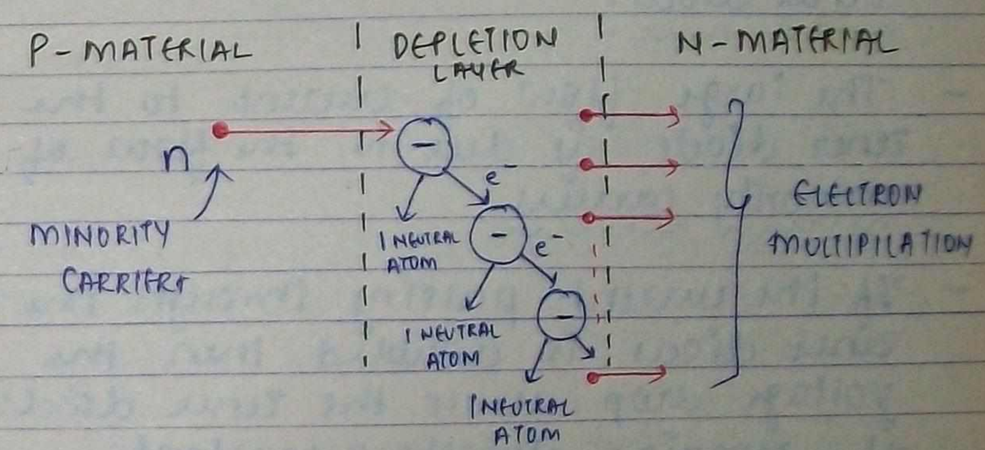
⊛

- Zener breakdown voltage decreases with the temp (NTC)
- The temp. coefficient of zener breakdown voltage is negative.

⊛ for avalanche to occur $V_{BR} > 6V$

⇒ AVALANCHE BREAKDOWN PHENOMENON – (IMACT IONISATION)





- It is due to electron multiplication.
- It is due to multiple collisonr between electrons and ions. in the depletion layer
- It is due to impact ionisation.
- Avalanche breakdown occur for breakdown voltages greater than 6V.

Now a days (*) No avalanche diode exist.

(*)

- Avalanche breakdown voltage increases with temp. (PTC).

- The temp. coefficient of avalanche breakdown voltage is positive.

NOTE -

- Impact ionisation occur in avalanche & zener diode.

- The large flow of current to the zener diode is due to the flow of minority carriers.

- If the current passing through the zener diode is doubled then the voltage drop across the zener diode is remains almost a constant.

- In a highly doped diode the breakdown is due to zener breakdown effect.

EXPLANATION -

(1) $\downarrow V_{Br} \propto \frac{1}{\text{DOPING} \uparrow}$

Smaller V_{Br} is $< 6V$
is zener effect

(2) DOPING $\uparrow$, $W \downarrow$, $\mathcal{E} \uparrow$

larger $|\mathcal{E}|$, hence zener effect

- In a lightly doped diode the breakdown is due to avalanche effect.

- $V_{Br} < 6V$ ZENER BREAKDOWN (NTC)

$V_{Br} = 6V$ (does not exist) ('0' TC)

$V_{Br} > 6$ AVALANCHE BREAKDOWN (PTC)

- when compare to avalanche breakdown, zener breakdown has higher doping conc.

- $V_{Br} < 4.5V$ Zener breakdown effect

4.5 V to 6V Zener or avalanche effect

$V_{Br} > 6V$ avalanche effect

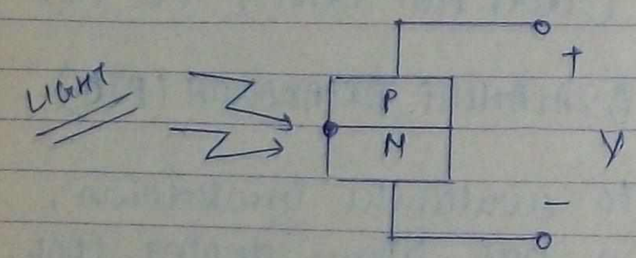
⇒ SOLAR CELL -

- It is a photovoltaic cell.

- PRINCIPLE -

PHOTO-VOLTAIC EFFECT.

- When light falls at the junction a small voltage is induced at the terminal and that voltage is called photovoltaic emf.



- The terminal voltage of a solar cell can be pratically measured by using a voltmeter.

- The terminal voltage of the solar cell cannot exceed contact potential of the diode.

- The terminal voltage of the solar cell is always less than contact potential of the diode

- The maximum solar cell voltage is
  $V = 0.1\,V$ for Ge diode.
  $V = 0.6\,V$ for Si diode.

- Solar cells are widely used in satellites.

- Solar cells are always operated under forward biased.

- Cutin voltage for the solar cell is zero volt.

FIELD EFFECT TRANSISTOR

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- The operation of the FET depends on electric field intensity produced in the channel.
- voltage controlled device (VCD)
- The other example for VCD are : vacuum tubes, OP-AMP, MOSFET.
- unipolar device.
- majority carrier device.
- minority carriers are zero (absent).
- Less noisy device due to the absence of minority carriers.
- leakage current are zero (due to the absence of minority carriers).
- Excellent thermal stability due to the absence of leakage current so that the temp. effect on the device is negligible and therefore very good thermal stability.
- when compare to BJT, FET is smaller in size and easier to fabricate.
- fabricated only with Si.
- Offset voltage is zero.
- FET can be used as a excellent signal chopper because of zero offset voltage.
- High input resistance device. (greater than 1 MΩ).
- Internal power consumption is negligible.
- FET amplifier can be designed without a self-biased arrangement and this is due to excellent thermal stability.
- Offers a larger bandwidth and therefore reproduction of input signal is excellent
- In FET Gain, bandwidth product (GBW) is a constant.

- DISADVANTAGES -

1. Smaller gain
2. Smaller GBW

(*) HIGHEST I/P RESISTANCE DEVICE – MOSFET

DE-MOSFET – DEPLETION-ENHANCEMENT – MOSFET

- when compare to BJT, FET is a better device as an amplifier.

- **SOURCE (S)** –
  It is the terminal by which magority carriers are entering into the device.

- **DRAIN (D)** –
  It is the terminal by which magority carriers will be leaving the device.

- **GATE (G)** –
  It is the terminal which controls the magority carriers moving from source to drain or indirectly control the drain current.

- **CHANNEL** –
  It is the region or space in between the two gates

- Source is analogus to Emitter
  Gate —— || —— Base
  Drain —— || —— Collector
  CS —— || —— CE
  CD —— || —— CC
  Source follower —— || —— Emitter follower.

(*) IGFET – insulated gate FET
MOST – metal oxide S.C. tx. (OR)
metal oxide silicon tx.

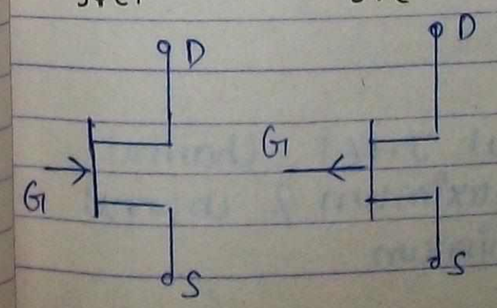
- FET is a symmetrical device and therefore source and drain terminals can be inter-changed practically.

- BJT is asymmetrical device and therefore emitter & collector terminals cannot be interchanged practically.

⇒ **CLASSIFICATION OF FET** –

FET

- JFET (JUNCTION FIELD EFFECT) TRANSISTOR
  - 3 TERMINAL DEVICE (S, G, D)
  - R_i is from 10^6 to $10^8 \Omega$
  - N-CHANNEL JFET
  - P-CHANNEL JFET



- MOSFET (METAL OXIDE S.C.) FET (IGFET) OR (MOST)
  - 4 TERMINAL DEVICE (S, G, D, SUB)
  - R_i is 10^{10} to $10^{15} \Omega$
  - DEPLETION MOSFET (DE MOSFET) → Suitable to operate both in depletion mode & enhancement mode
  - ENHANCEMENT MOSFET (E-ONLY MOSFET) → Suitable to operate only for enhancement mode

- Pre existing channel is available in DE MOSFET. There is no pre existing channel in E MOSFET.

- The channel has to be created by applying proper gate to source voltage (V_{GS}) in E-MOSFET.

NOTE -

- R_i of MOSFET > R_i of JFET
- P_D of MOSFET < P_D of JFET
- IGFET stands for
  - (A) insulated gate FET
  - (B) isolated gate FET
  - (C) integrated gate FET
  - (D) current controlled gate FET

- In MOSFET the gate is isolated by using SiO_2 layer but the device is defined as insulated gate FET.

⇒ N-CHANNEL J-FET -

- In unbiased n-channel J-FET channel cross sectional area is maximum & channel current density is minimum.

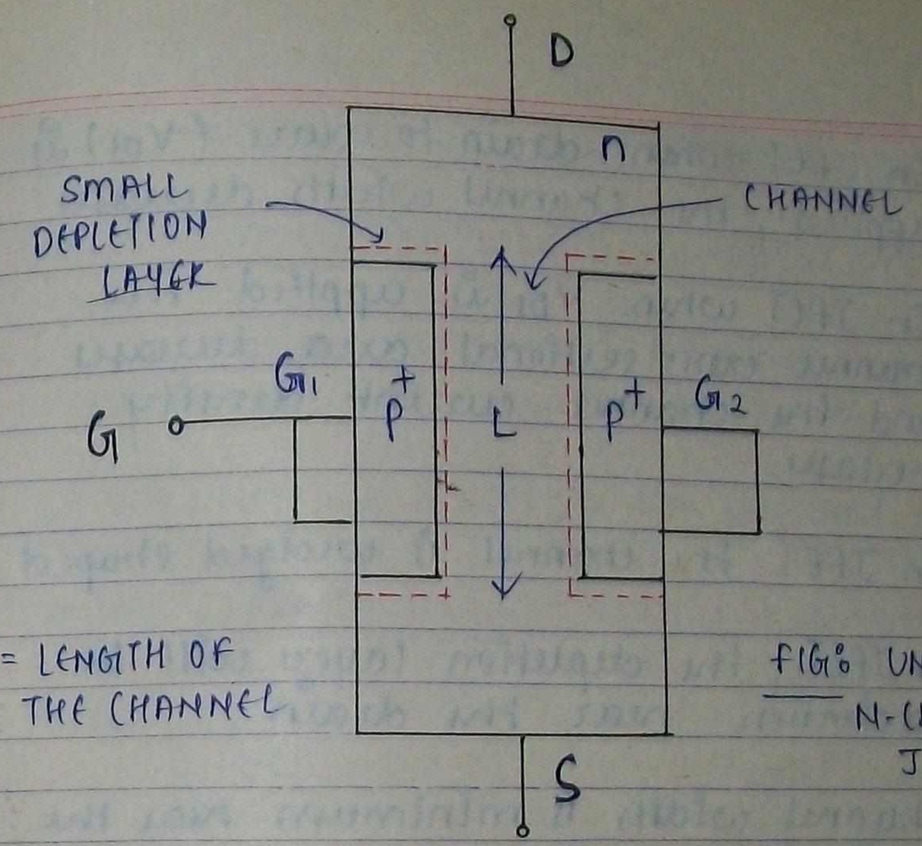
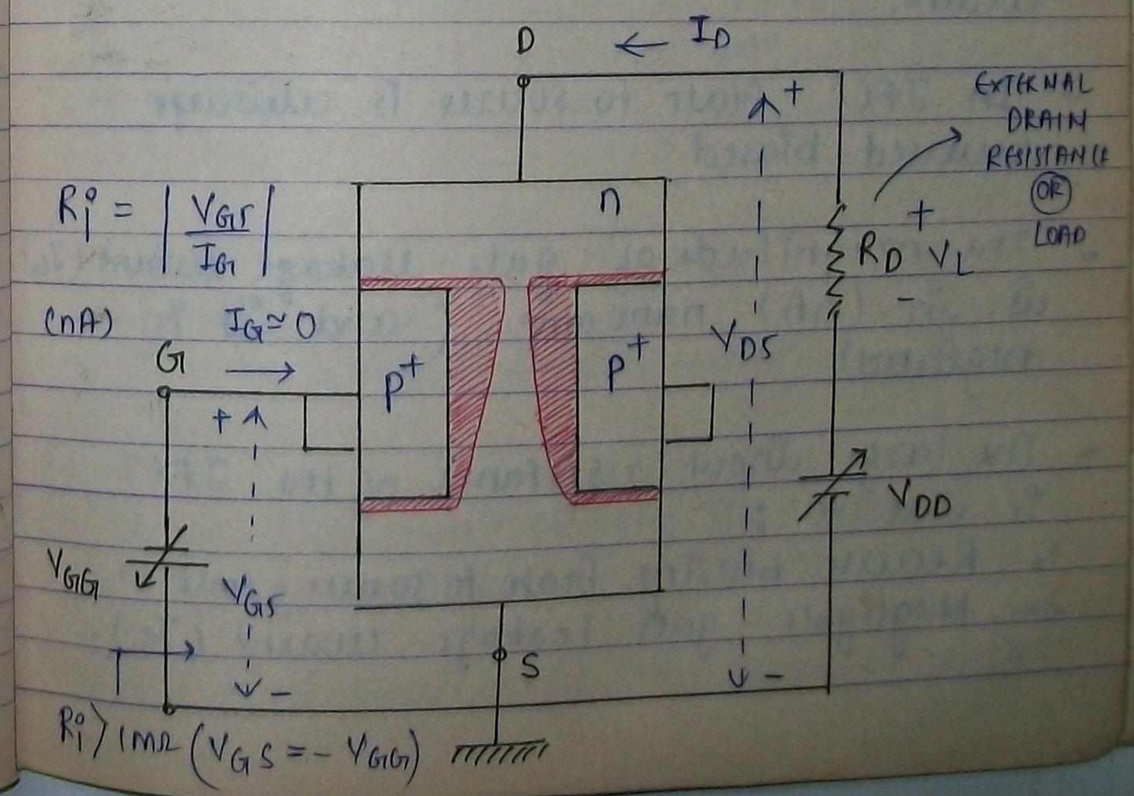


FIG: UNBIASED N-CHANNEL JFET



- In JFET when drain to source (V_{DS}) is applied, the channel width decreases.

- In JFET when V_{DS} is applied the channel cross sectional area decreases and the channel current density increases.

- In JFET the channel is wedged shaped.

- In JFET, the depletion layer will be maximum near the drain.

- Channel width is minimum near the drain.

- In JFET Gate to source is always reversed biased.

- The magnitude of gate leakage current (I_G) is in (nA) nanoamp. (and it is neglected)

- The large input resistance of the JFET is due to:
  1. Reverse biasing Gate to source junction
  2. Negligible gate leakage current (I_G).

- In n-channel JFET, gate voltage is negative.

- for P-channel JFET, gate voltage is positive.

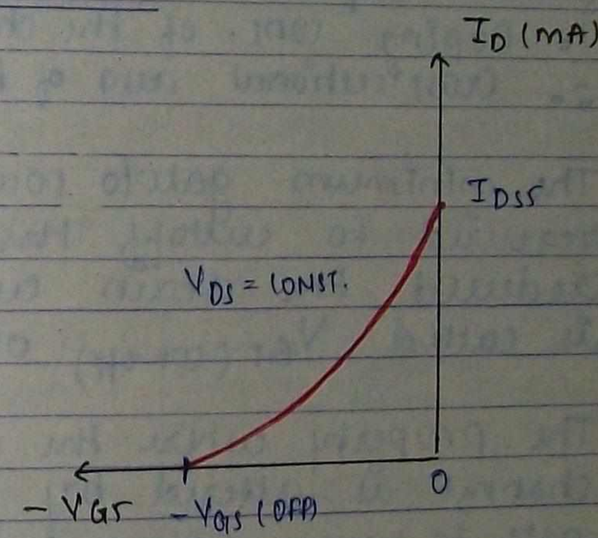
- In FET, I/P characteristic cannot be plotted because the I/P current is $I_G \simeq 0$.

(1) BY VARYING V_{GS} & KEEPING V_{DS} CONSTANT –

TRANSFER CHARACTERSTICS:

I_D Vs V_{GS} | V_{DS} = CONST.

FOR N-CHANNEL JFET:



- The maximum drain current in JFET is I_{DSS}

- I_{DSS} = Drain to Source Safe current (OR)
  = Drain to Source Saturation current

- In N-channel JFET if gate is given

more negative voltage then I_D decrease.

- In JFET when gate to source is more reversed biased, the channel width decreases and their majority carriers will be reaching the drain, and I_D decrease.

- The conc. of majority carriers in the channel depends on :
  1. Doping conc. of the channel.
  2. Cross sectional area of the channel.

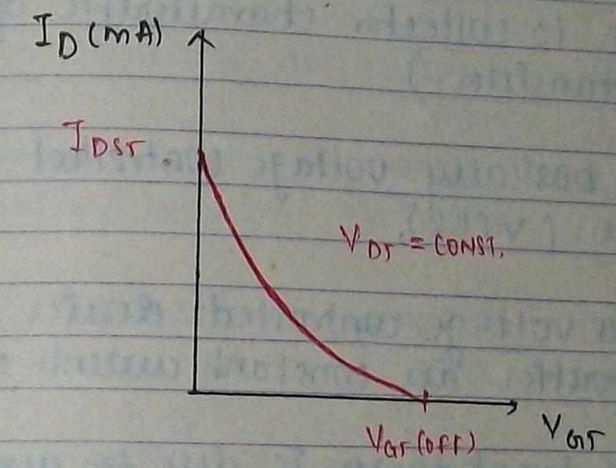
- The minimum gate to source voltage required to cutoff the channel or reduced the drain current to zero is called $V_{GS(cut\text{-}off)}$ or $V_{GS(off)}$.

- The property where the width of the channel is altered by varying the gate to source voltage is called CHANNEL WIDTH MODULATION.

- Channel width modulation is similar to base width modulation in the BJT.

- Channel width modulation can be seen in the JFET, D-MOSFET & E-MOSFET.

- The transfer characteristic for p-channel JFET is given below.

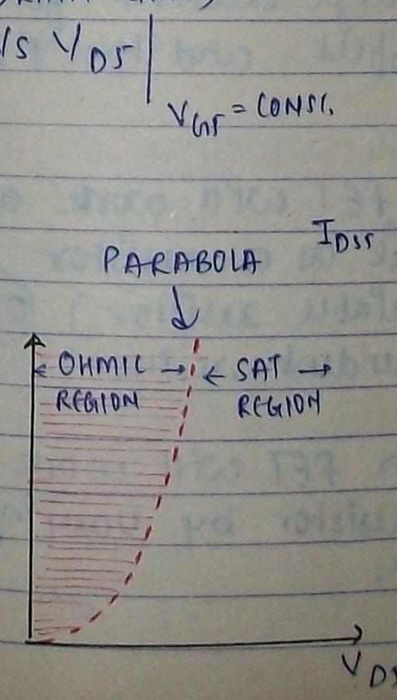


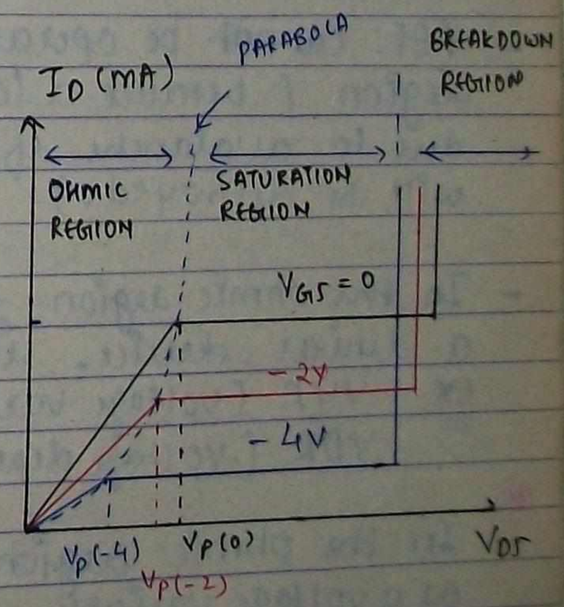
(2) BY VARYING V_{DS} & BY KEEPING V_{GS} CONSTANT -

OUTPUT CHARACTERISTICS :

(OR) (DRAIN CHAR.)

I_D Vs V_{DS} | V_{GS} = CONST.





- The drain characteristic of FET is called constant current characteristic (and it is similar to collector characteristic of common base transistor.)

- FET is basically voltage controlled current source (VCCS).

- FET is a voltage controlled device but its characteristics are constant current characteristics.

- In FET breakdown is due to avalanche effect.

- FET cannot be operated in the breakdown region (because a large current flows due to avalanche effect and the FET will be destroyed.)

- In the ohmic region FET will work as a linear device, ie as a resistor
  Ex - VVR (voltage variable resistor) or
  VDR (voltage dependent resistor)

- In the ohmic region FET will work as a voltage variable resistor by varying gate to source voltage.

- Ohmic region is also called linear region or non-saturation region.

- In JFET channel behaves as a resistor.

- Saturation region is called current-saturation region or pinch off region

- In the saturation region FET will work as a ON SWITCH and also as an AMPLIFIER.

- FET is generally operated in saturation region.

- In the pinch off region if V_{DS} is increasing then the drain I_D will remain almost a constant.

- FET is generally operated with:
  1. $V_{DS} = V_P$
  2. $V_{DS} >> V_P$
  3. $V_{DS} < V_P$
  4. $V_{DS} > V_P$

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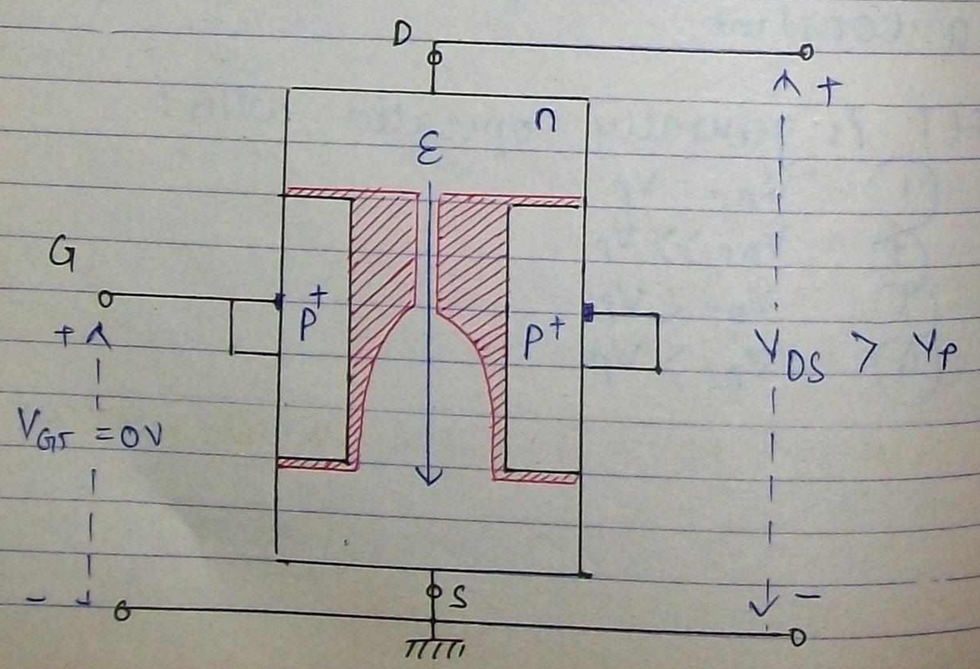
⇒ PINCH OFF VOLTAGE (V_P) -

- Pinch off voltage is defined as the minimum drain to source voltage where I_D enters into saturation.
- Pinch off voltage is a function of V_{GS}.
- The max. pinch off voltage is $V_{P(0)}$ or V_{P0}.
- In a JFET when V_{GS} is applied, the pinch off voltage is reduced.
- The locus of the pinch off voltage correspond to a parabola.



- In JFET during the pinch off both the depletion layers will be coming extremely closer but they cannot touch with each other and this is due to the larger electric field intensity near the drain and pointing towards the source.

⊛ NOTE -

- The larger electric field intensity will be preventing the two depletion layer from touching with each other
- During the pinch off the depth of the depletion layer will be very narrow but the drain voltage is very large & highly positive and it will be attracting maximum electrons from the channel and therefore the drain current will remain almost a constant

⊛

- The drain is attracting the maximum electron from the channel with higher kinetic energy.

⇒ GENERAL EQUATION FOR DRAIN CURRENT -

- In the saturation region of FET :

$$\boxed{I_D = I_{SS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

V_{GS} & V_P must have same sign

- FET is a square law device.

- In JFET, I_D decreases as a parabolic variation with V_{GS}.

- Drain current is a majority carrier current.

- I_D decreases with the temperature ($\mu \downarrow$)

- For 1°C, I_D decreases by 0.6 %.

- As temp. increases mobility of charge carrier decreases hence I_D decreases with the temp.

- FET is having excellent thermal stability and this is due to :
  1. Absence of leakage current.
  2. As temp. increases I_D decreases.

- Drain current is a drift current because this current is passing through the channel under the influence of electric field intensity

- In FET -	In BJT -
$I_D \downarrow$ with T	$I_C \uparrow$ with T
Hence $R \uparrow$ with T	$R \downarrow$ with T
∴ FET has PTC of resistance	∴ BJT has NTC of resistance

(*) $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{|V_{GS(cut\text{-}off)}|}\right]^2$$

⇒ **RELATIONSHIP B/W V_P & $V_{GS(CUTOFF)}$ -**

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{|V_P|}\right]^2$$

V_{GS} & V_P must have same sign.

If $V_{GS} = V_P$ then $I_D = 0$

V_{GS} → $V_{GS(CUT\text{-}OFF)}$. V_P → max I_D $I_D = 0$ → condition for cutoff

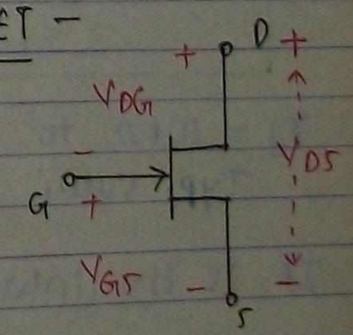
∴ In N-channel JFET

(*) $$\boxed{V_P = \left|-V_{GS(CUTOFF)}\right|}$$

- In FET $V_{GS(cutoff)}$ is $-8V$, then V_P is $+8V$

⇒ **TERMINAL VOLTAGES OF FET -**

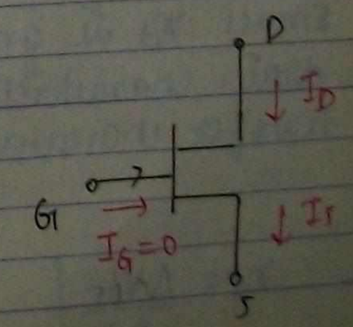
$$\boxed{V_{DS} = V_{DG} + V_{GS}}$$



⇒ **SOURCE CURRENT -**

$$\boxed{I_D \equiv I_S}$$

in magnitude.



⇒ GENERAL EQ^n FOR GATE TO SOURCE VOLTAGE –

Since, $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

therefore, $\boxed{V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]}$

⇒ FET PARAMETERS –

I_D is a $f(V_{GS} \& V_{DS})$

(1) DRAIN RESISTANCE (r_d) –

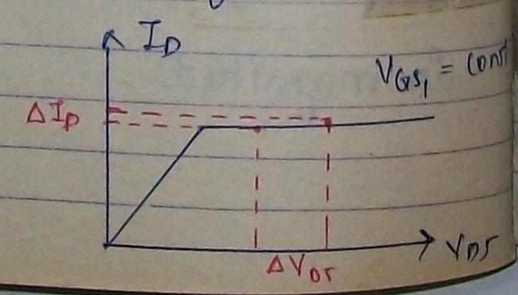
$$\boxed{r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{CONST.}}}$$

$r_d = 10\,k\Omega$ to $600\,k\Omega$

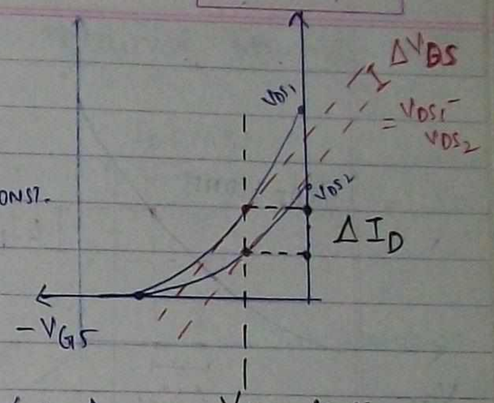
Typ. value $= 500\,k\Omega$

- It is the internal resistance of FET.
- Small r_d is graphically obtained from drain characteristic and also from the transfer characteristics.

$$\therefore\ r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\ \text{CONST.}}$$



$$\therefore\ r_D = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\ \text{CONST.}}$$

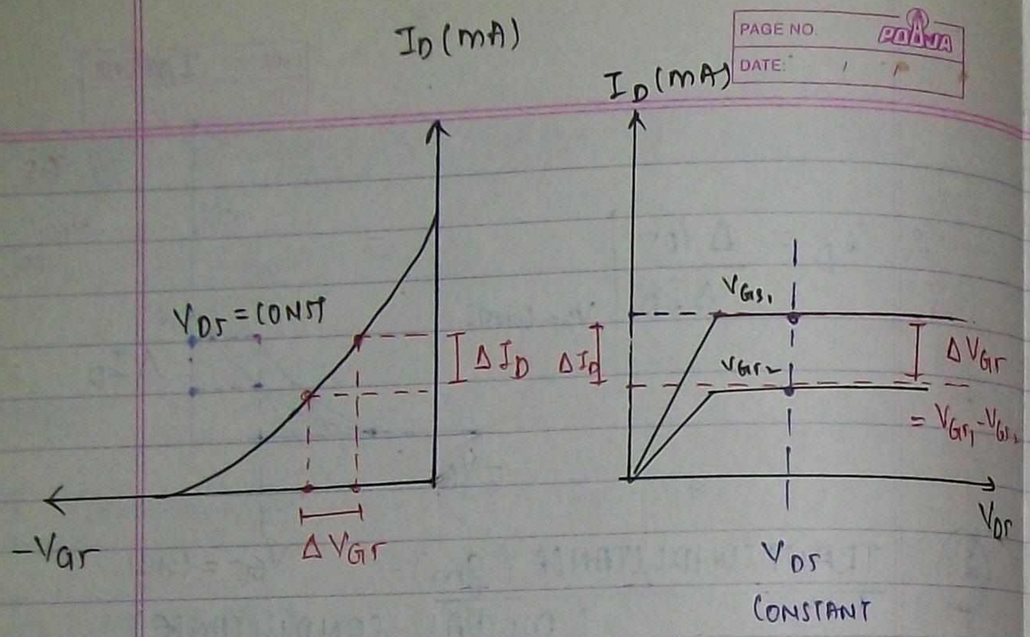


(2) TRANSCONDUCTANCE (g_m) –
(MUTUAL CONDUCTANCE).

$$\boxed{g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS} = \text{CONST.}}}$$

	JFET	MOSFET	BJT
g_m =	0.1 mS to 10 mS	0.1 mS to 20 mS	50 mS to 600 mS

- In any device, Gain, $|A| \propto g_m$.
- Gain is small in the FET because of smaller value of g_m.
- g_m is graphically obtained from transfer characteristic and also from drain characteristics.



③ AMPLIFICATION FACTOR (μ) —
(VOLTAGE AMPLIFICATION FACTOR)

$$\boxed{\mu = -\left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)\Bigg|_{I_D = \text{CONST.}}}$$

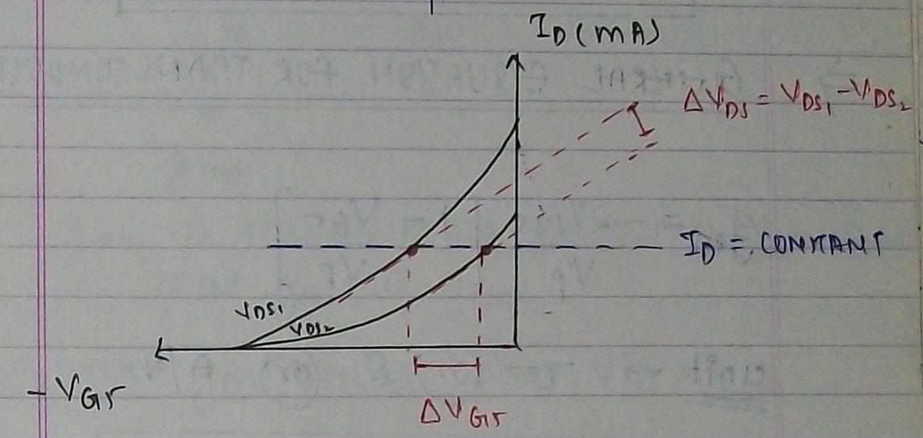
- μ = 2.5 to 150
- μ is the most important specification of the FET.
- The max. voltage gain of the FET is given by μ.

$$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)\Bigg|_{I_D = \text{CONST}}$$

(OR)

$$\mu = -\frac{V_{DS}}{V_{DS}}\Bigg|_{I_D = \text{CONST}}$$

- μ is graphically obtained from transfer characteristic only:



- In FET always $\mu = r_d \times g_m$

⇒ **DERIVE AN EQUATION FOR TRANSCONDUCTANCE IN FET -**

- In saturation region of FET -

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

By defination,

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Bigg|_{V_{DS} = \text{CONST}}$$

Differentiating the above equation wrt V_{GS}.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Bigg|_{V_{DS}} = -\frac{2 I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$\boxed{g_m = \frac{-2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]} \ \mho$$

⇒ GENERAL EQUATION FOR TRANSCONDUCTANCE -

$$g_m = \frac{-2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]$$

unit → $\mho$ (or) S (or) A/V.

from eqn of I_D -

$$\left[1 - \frac{V_{GS}}{V_P}\right] = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = \frac{-2I_{DSS}}{V_P}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$\boxed{g_m = \frac{-2}{V_P}\sqrt{I_{DSS} \cdot I_D}}$$

let $I_D = I_{DS}$

$$\boxed{g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} \cdot I_{DS}}}$$

Now,

If $V_{GS} = 0$,

$$g_m = \frac{-2I_{DSS}}{V_P} \ \mho$$

$\downarrow$

g_{mo}

g_{mo} is the value of g_m when $V_{GS} = 0$.

∴ max g_m is g_{mo}.

∴ max g_m occurs when $V_{GS} = 0$

$$\boxed{\text{Max } g_m \text{ or } g_{mo} = \frac{-2I_{DSS}}{V_P}} \ \mho$$

max. pinch off voltage = V_{PO} (or) internal pinch off voltage

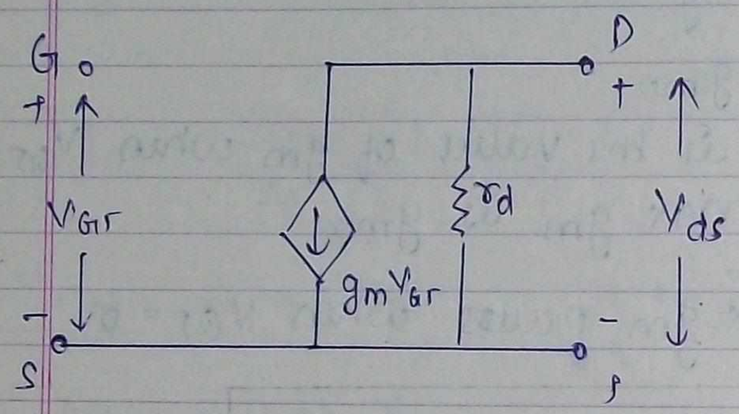
$$\boxed{V_{PO} = \frac{-2I_{DSS}}{g_{mo}}} \text{ volts.}$$

$$\therefore \boxed{g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right]} \ \mho$$

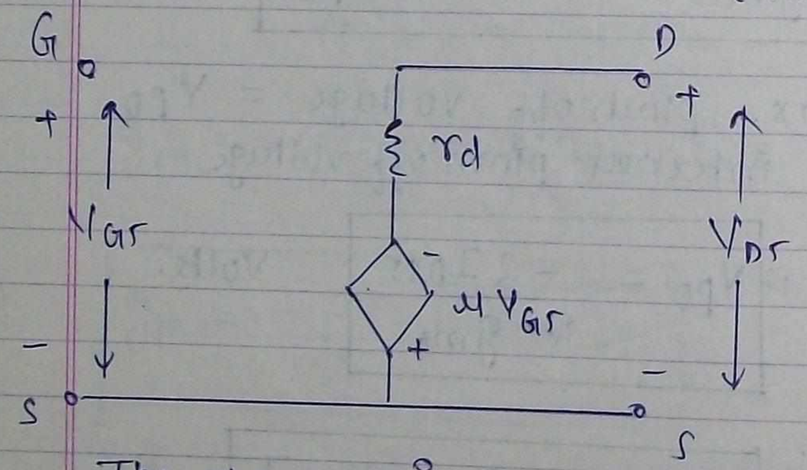
$$\boxed{g_m = g_{mo}\sqrt{\frac{I_D}{I_{DSS}}}} \ \mho$$

⇒ EQUIVALENT CIRCUT OF FET (JFET & MOSFET) -

① CURRENT SOURCE EQUIVALENT - (NORTON EQ.)



② VOLTAGE SOURCE EQUIVALENT - (THEVENIN EQ.)

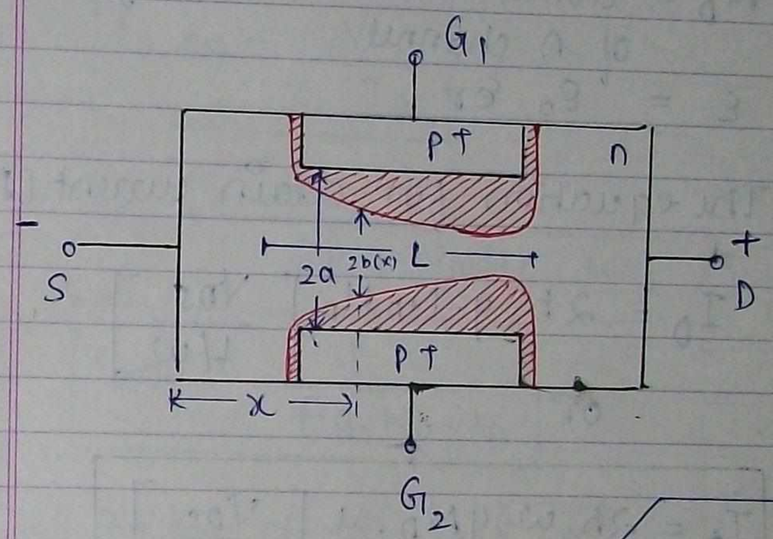


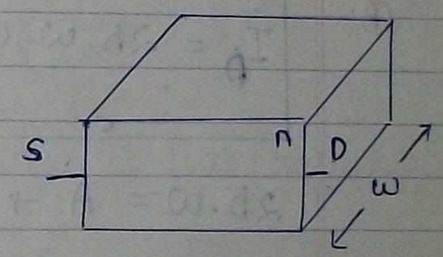
$(\mu = g_m r_d)$

- The above circuits are called LOW FREQUENCY and small signal equivalent circuit of the FET. (OR) AC equivalent circuit of the FET. and they are used to calculate the voltage gain and output resistance of the FET amplifier.

⇒ GENERAL EQUATIONS FOR JFET -

- Considering N-channel JFET





L = Length of the channel.

W = width of the channel.

2a = Actual channel width before the penetration of depletion layers.

a = half channel width befor the penetration of depletion layers.

x = distance measured from source end.

2b(x) = channel width after the penetration of depletion layers measured at the distance x.

The eqn for pinch of Voltage. (V_{PO}) (OR) internal pinch-off voltage (V_P)

$$\boxed{|V_P| = \frac{q \cdot N_D \cdot a^2}{2\varepsilon}}$$ volt.

N_D = donar conc. or doping conc. of n channel

$\varepsilon = \varepsilon_0 \cdot \varepsilon_r$

- The equation for drain current (I_D)

$$I_D = 2b \cdot q \cdot N_D \mu_n \left[\frac{V_{DS}}{L/w} \right]$$

or

$$\boxed{I_D = 2b \cdot w \cdot q N_D \cdot \mu \left[\frac{V_{DS}}{L} \right]}$$

$2b \cdot w = A$ → area of cross section of the channel.

$$\boxed{I_D = A q N_D \mu \left[\frac{V_{DS}}{L} \right]}$$

Thus,

$I_D \propto w/L$

$I_D \propto V_{DS}$

$I_D \propto A$

$I_D \propto N_D$

DRAIN TO SOURCE RESISTANCE –

- The drain to source resistance (r_{DS}) or channel resistance or $r_{d,ON}$ –

$$\boxed{r_{d,ON} = \frac{V_{DS}}{I_D}} \ \Omega$$

$$r_{d,ON} = \frac{1}{2b \cdot q \cdot N_D \mu_n \left(\frac{w}{L}\right)}$$

$$\boxed{r_{d,ON} = \frac{L}{Aq \cdot N_D \mu_n}}$$

$r_{d,ON} \propto L/w$ }

- $r_{d,ON}$ is in the range of 100Ω to 100kΩ
- $r_{d,ON}$ is the important parameter in switching applications of FET.

$$\boxed{R_i \text{ of BJT} < r_{d,ON} \text{ of FET.}}$$

- Internal pinch off voltage (V_{po})

$$\boxed{V_{po} = V_{bi} + V_P}$$

V_{bi} = built in potential of the PN junction diode.

$$V_{bi} = V_T \log_e \left(\frac{N_A N_D}{n_i^2} \right)$$

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⇒ When JFET is operated in ohmic region:

$$\boxed{V_{DS} = V_p + V_{GS}}$$

Que. What is the max voltage gain obtain from FET having $g_m = 5mS$ and $r_d = 10k\Omega$

Solⁿ: Max. voltage gain.

$$\mu = g_m \cdot r_d$$
$$= \underline{\underline{50}}.$$

Que. What is the max. transconductance for a JFET having $I_{DSS} = 8mA$ & $V_p = -4V$.

Solⁿ: max $g_{mo} = \dfrac{-2I_{DSS}}{V_p}$

$$= \underline{\underline{4\,mS}}$$

Que. Calculate the g_m for a JFET having $I_{DSS} = 8mA$ $V_p = -4V$ and is biased to operated at $V_{GS} = -1.8V$.

Solⁿ:
$$g_m = \frac{-2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]$$
$$= 4\times10^{-3}(2.2/4) = \underline{\underline{2.2\,mS}}$$

Que. When gate to source voltage of FET changes from $-3V$ to $-3.1V$ I_D changes from $1.3mA$ to $1mA$, assuming other parameter to be constant find g_m?

Solⁿ:
$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = 3\,mS$$

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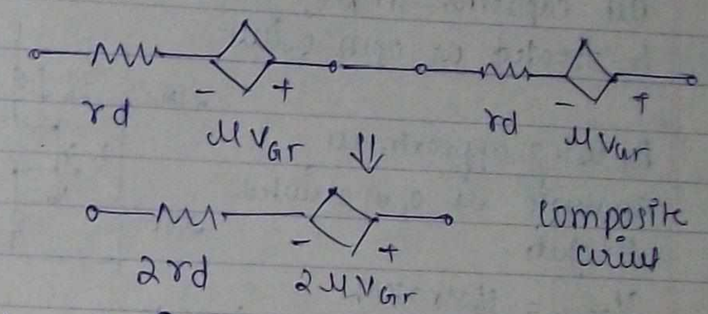
Que. If 2 identical FETs each having μ (amp. factor) and drain resistance (r_d) are connected in series for the composite circuit. Find its amp. factor and drain resistance.

Solⁿ:



New drain resistance $= 2r_d$

New amp. factor $= 2\mu$

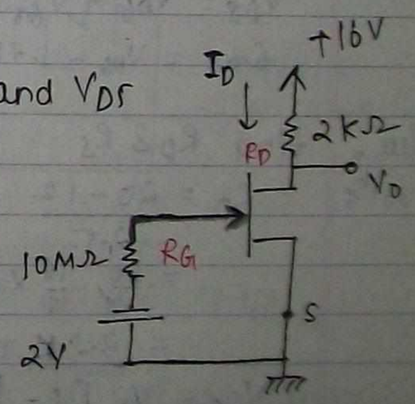
Que. Two identical FET having g_m and r_d are connected in parallel, for the composite circuit find its g_m' and r_d'

Solⁿ: $r_d' = \dfrac{r_d}{2}$, $g_m' = 2g_m$

Que. Calculate V_{GS}, I_D and V_{DS}

Given $I_{DSS} = 10mA$

$V_p = -8V$



Solⁿ: Since $I_G = 0$,

$$V_{GS} = \underline{\underline{-2}}$$

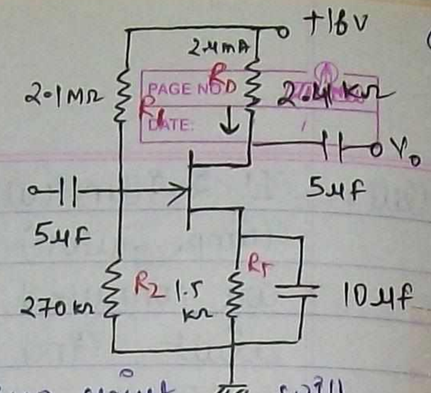
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

$$I_D = \underline{\underline{5.625\,mA}}$$

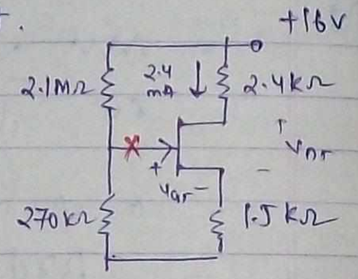
$$V_{DS} = V_D$$
$$= V_{DD} - I_D R_D$$
$$= 16 - 5.625\times2$$
$$= 4.75V$$

Que. Calculate V_{GS}, V_{DS}, V_{DG}

Solⁿ: terminal voltage of FET can be calculated under dc analysis & all capacitor in the given circuit will be treated as open circuit.



By using approximate analysis we open circuited the gate.



$$V_{270k} = \frac{16V \times 270k}{2.1M + 270k} = 1.82V$$

$I_D = I_S = 2.4mA$

$V_{270} = V_{GS} + I_S R_S =$

$1.82 = V_{GS} + 2.4\times10^{-3} \times 1.5k$

$V_{GS} = -1.78$ Volts

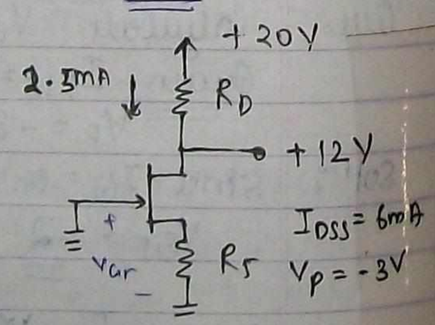
$V_{DS} = V_{DD} - I_D(R_S + R_D) = 6.64V$

$V_{DS} = V_{DG} + V_{GS}$

$6.64 = V_{DG} - 1.78$ $\quad V_{DG} = 8.42$ Volts

Que. find R_D & R_S

Solⁿ:



$$R_D = \frac{20-12}{2.5} \times 10^3$$

$$= \frac{16}{5} \times 10^3$$

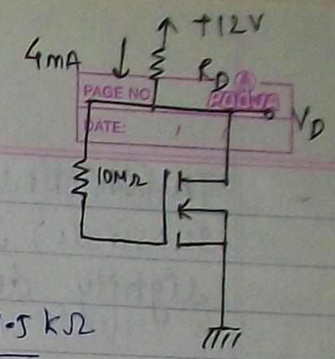
$$= 3.2 k\Omega$$

$$V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{SS}}}\right] = -1.06V$$

$$R_S = \left|\frac{V_{GS}}{I_S}\right| = 442\Omega$$

Que. Given $V_D = \frac{V_{DD}}{2}$, find R_D

Solⁿ:

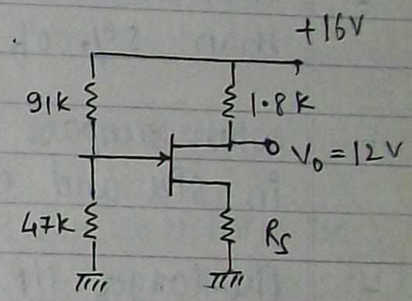


$V_D = 6V$

$R_D = (12-6)/4 = 6/4 = 1.5 k\Omega$

Que. If $V_{GS} = -2V$, find R_S.

Solⁿ:



$$I_D = \frac{16-12}{1.8} \times 10$$

$= 2.2 mA$

$$V_{47k} = \frac{16 \times 47k}{91k + 47k}$$

$= 5.44V$

$5.44 = V_{GS} + I_D R_S$ $\quad R_S = 3.35 k\Omega$

MOSFET -

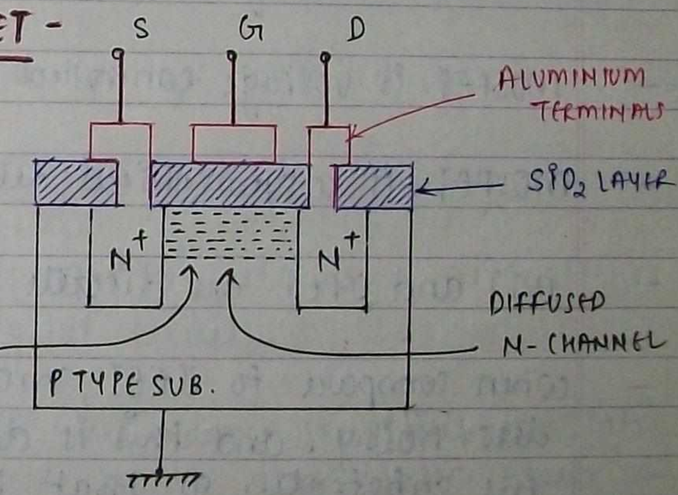


FIG: DE-MOSFET (N-CHANNEL)

- An integrated circuit or S.C. chip.
- fabricated with VLSI by using planar technology.

- The thickness of Si wafer (used as a substrate) is 0.5 μm. and it is lightly doped.
- The entire area of the MOSFET is less than 5% of the area required for BJT.
- when compare to JFET MOSFET are smaller in size and easier to fabricate.
- The larger I/P resistance of the MOSFET is due to SiO_2.
- The thickness of SiO_2 layer is 1000Å - 2000Å unit.
- MOSFET is voltage controlled device (VCD).
- MOSFET is a symmetrical device
- BJT and JFET are discrete components
- when compare to JFET, MOSFETs are less noisy. and this is due to grounding the substrate. so that the noise level in the device can be filtered out
- In DEMOSFET, there is a ~~pre~~ existing channel.
- In DE-MOSFET channel is diffused channel.
- In the gate region, the layers are metal, - oxide - S.C layer and hence called MOSFET.
- MOSFET is basically a capacitor.
- A parallel plate capacitor will be formed at the gate region with Al+ plate and S.C. channel are the two plates of the capacitor. & SiO_2 as the dielectric.
- MOSFET is voltage controlled capacitor (VCC).
- Ideal MOSFET is VCC.
- MOSFETs are widely used as switches in digital circuits.
- MOSFETs are very sensitive to static electrical noise and static electrical disturbences.
- MOSFET is faster than JFET
- BJT is faster than MOSFET.

- JFET is always operated under depletion mode.

- In BJT there will be a minority carrier storage time.

- In MOSFET minority carrier storage time is zero (because there are no minority carriers).

- In MOSFET since minority carrier storage time is zero, the turn off time of device is very small, hence MOSFET is more suitable for high freq. applications, when compare to the BJT.

- DEPLETION MODE: max $I_D \rightarrow I_{DSS}$; $\boxed{I_D \leq I_{DSS}}$

  ENHANCEMENT MODE: min $I_D \rightarrow I_{DSS}$; $\boxed{I_D \geq I_{DSS}}$

- JFET is operated under depletion mode.

- N channel DEMOSFET is sometimes called dual MOSFET because it is suitable for both depletion mode & enhancement mode.

- P channel depletion MOSFET is generally used for enhancement mode.

- NMOS is faster than PMOS because $\mu_n > \mu_p$.

- PMOS is easier to fabricate

- PMOS is bulky and economical

- To get equal performance between PMOS and NMOS, PMOS require twice the area required for NMOS.

- The main advantage of NMOS is higher package density (ie it can store large amount of information in smaller area).

- CMOS - (Complementary MOSFET)

- CMOS is a combination of PMOS & NMOS.

- Input resistance $R_i = 10^{15}\,\Omega$.

- CMOS will not consume any power (this is the greatest advantage)

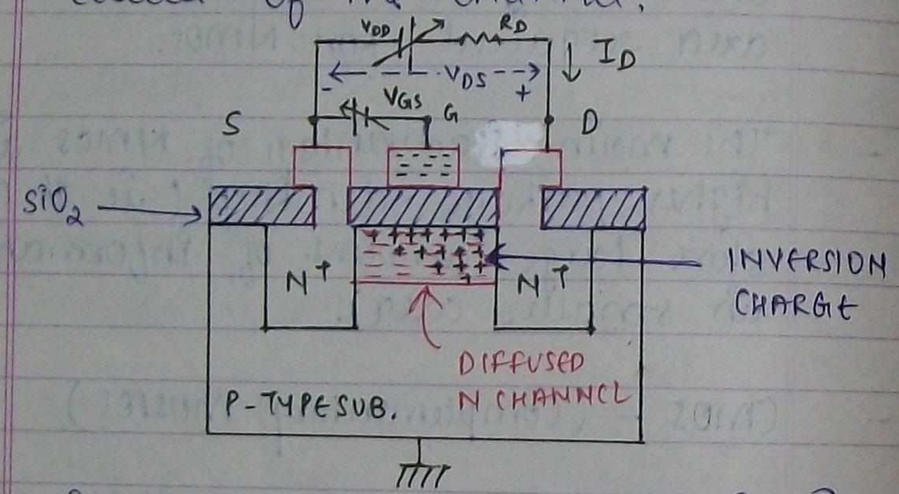
- CMOS is widely used as inverter.

- In CMOS inverter, whatever be the I/P signal one transistor is on the other is OFF.

31/7/11

⇒ OPERATION OF N CHANNEL DE-MOSFET UNDER DEPLETION MODE -

The principle of depletion mode is the applied gate to source voltage must induce majority carrier of the channel.



- for n-channel MOSFET drain is positively biased wrt source and to operate under depletion mode, gate is negatively biased with refrence to the source.

NOTE - In n-channel depletion MOSFET:
1. channel potential increases from source to drain.
2. charge Inversion charge increases from source to drain

∴ when V_{GS} is kept zero:

① WHEN $V_{GS} = 0$,

The gate is provided with zero and therefore the inversion charge is zero, hence max. number of electrons will be moving from source to drain and drain current is max. and is denoted by I_{DSS}. (Drain to source safe current).

② WHEN V_{GS} IS APPLIED -

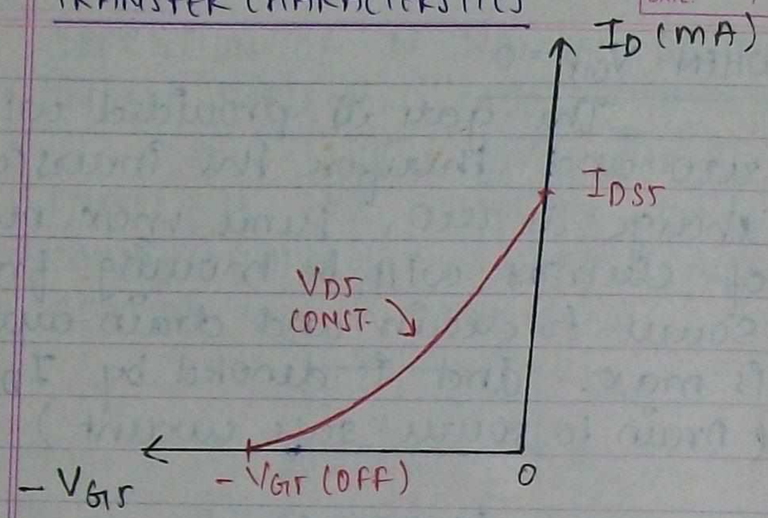
The gate is provided with a negative voltage and therefore positive charges are created in the diffused channel and due to the recombinations less negative charges will be reaching the drain, hence I_D decreases.

I_D further decreases if gate is given with more negative voltage.

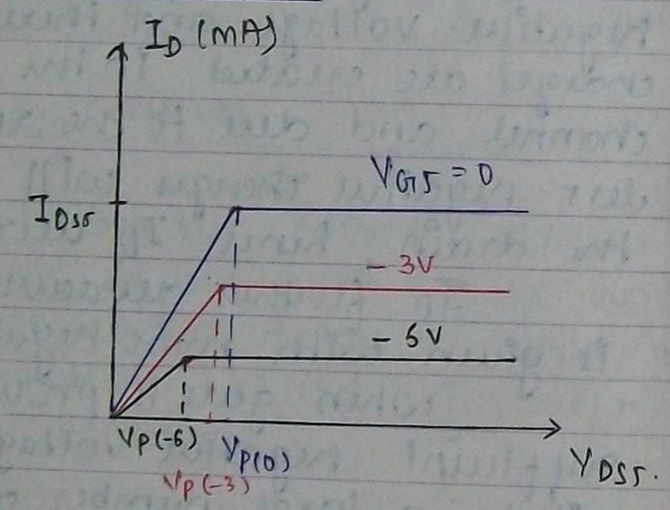
when gate is provided with sufficient negative voltage there will be a large number of positive charges created in the diffused channel resulting a total recombination. Hence, no electron will be reaching the drain and I_D reduces to zero, the channel is cutoff.

The transfer characteristic & drain characteristic for the n channel depletion MOSFET under depletion mode is given below:

① TRANSFER CHARACTERSTICS –



② DRAIN CHARACTERSTICS –



The eqn for drain current for the MOSFET operating under depletion mode is given by:

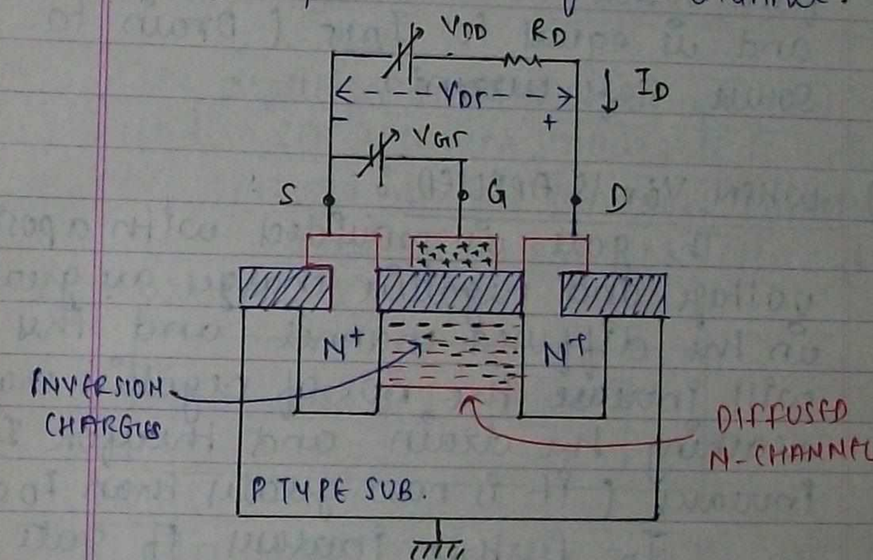
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{ Amp.}$$

NOTE – In above eqn V_{GS} & V_P must be having same sign (polarity).

– The above eqn indicate I_D decreases as a parabolic variation with V_{GS}.

⇒ OPERATION OF N CHANNEL DE-MOSFET UNDER ENHANCEMENT MODE –

The principle of enhancement mode is the applied gate to source voltage must increase the majority carriers of the channel.



for N channel MOSFET, drain is positively biased with reference to the source and to operate under enhancement mode, gate is positively biased with reference to the source.

NOTE – In n-channel DE-MOSFET:

1. Channel potential increases from source to drain.

2. Inversion charge increases from source to drain.

① WHEN V_{GS} IS KEPT ZERO:

The gate is now provided with a zero voltage and therefore the inversion charge is zero & minimum no of negative charge will be moving from source to drain and I_D is min. and is equal to I_{DSS} (Drain to source saturation current).

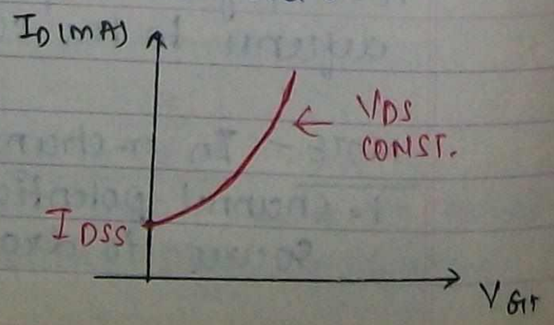
② WHEN V_{GS} IS APPLIED:

The gate is provided with a positive voltage and negative charges are greater in the diffused channel and this will increase the no. of negative charge reaching the drain and therefore I_D increases (it is now greater than I_{DSS}).

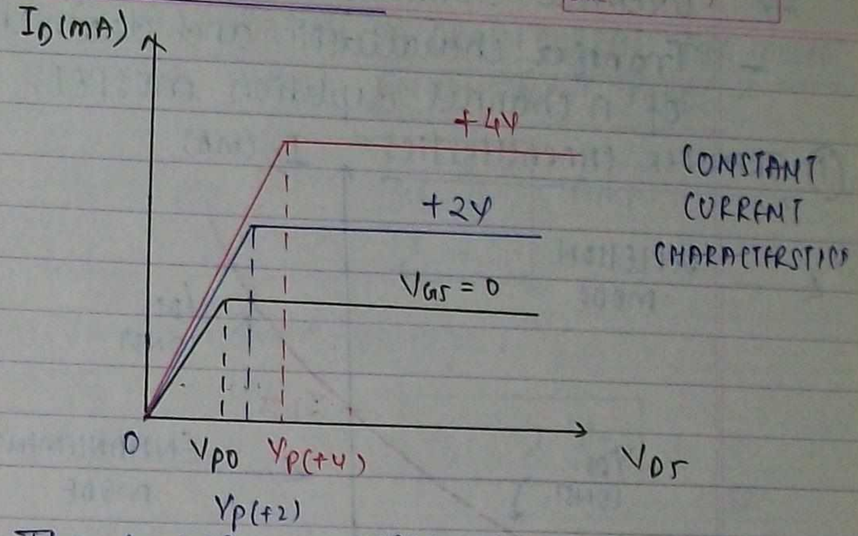
I_D further increases if gate is given with more positive voltage.

The transfer characteristic and drain chara. for n-channel DEMOSFET under enhancement mode are:

① TRANSFER CHARACTERSTICS-



② DRAIN CHARACTERSTICS -



The depletion mosfet when operated under enhancement mode, it is said to be operated in the pinch off condition.

Under pinch off condition drain current is:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

NOTE-

In above eqn V_{GS} and V_P will be having opposite sign.

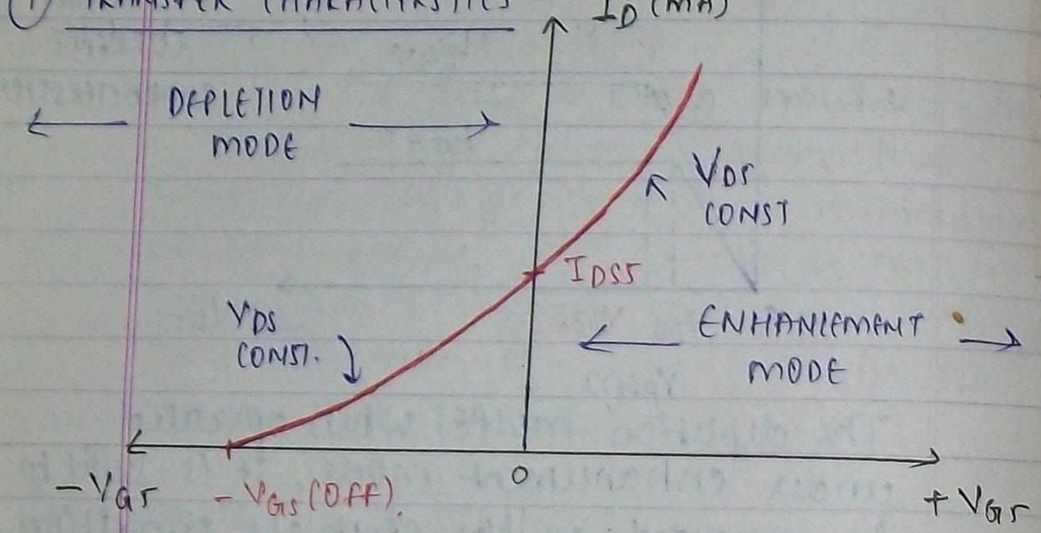
- The above eqn indicates the MOSFET drain current I_D increases as a parabolic variation with V_{GS}.
- Under pinchoff condition the minimum value of V_{DS} required is:

$$\min V_{DS} = V_P + V_{GS}$$

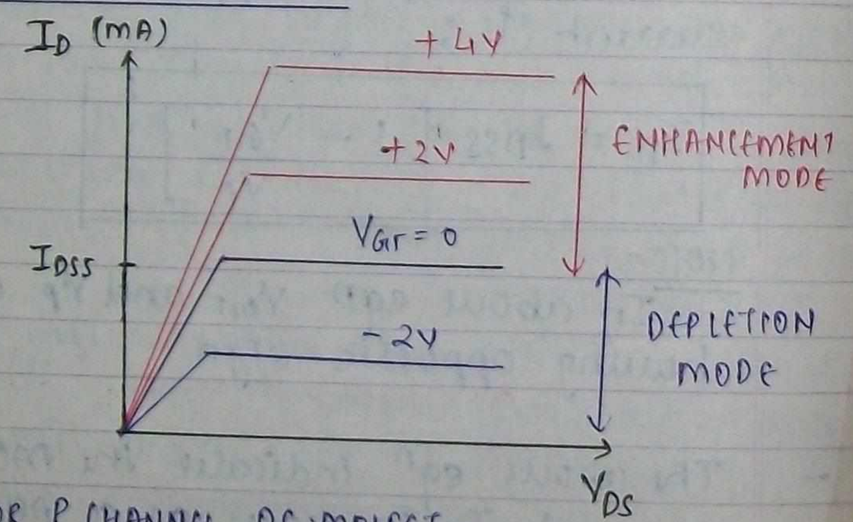
⇒ OVERALL CHARACTERSTICS —

- Transfer characteristic and drain characteristics of n channel depletion mosfet.

① TRANSFER CHARACTERSTICS —



② DRAIN CHARACTERSTICS —



(*) FOR P CHANNEL DE MOSFET —

1. Transfer chara. is mirror image about about y axis of N channel demosfet
2. Drain characteristic will remain same in 1st quad. but value of V_{GS} will change from +ve → -ve and -ve → +ve.

⇒ GENERAL EQUATION OF DRAIN CURRENT FOR MOSFET OPERATING UNDER ENHANCEMENT MODE —

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_T}\right]^2} \text{ Amp.}$$

V_T = threshold voltage.

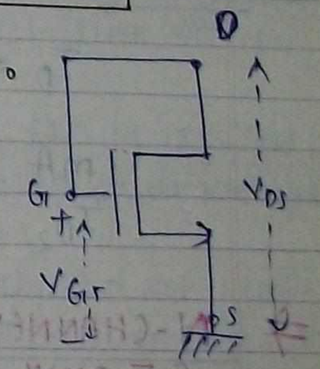
NOTE — when,

$$\boxed{V_{GS} \gg V_T}$$

Que. WORKBOOK P-26 Q-19.

Sol^n: Since G & D are shortcircuited.

$V_{GS} = V_{DS}$



MOSFET is in the ON state (or) ON switch i.e SAT. REGION.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_T}\right]^2$$

① method:

$$I_D \propto \left(1 - \frac{V_{GS}}{V_T}\right)^2$$

$$1mA \propto \left(1 - \frac{2}{1}\right)^2 \quad -①$$

$$I_{D_2} \propto \left(1 - \frac{3}{1}\right)^2 \quad -②$$

$$I_{D_2} = \underline{\underline{4mA}}$$

② Method: $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_T}\right]^2$

$$1\,mA = I_{DSS}\left(1-\frac{2}{1}\right)^2, \quad I_{DSS} = \underline{\underline{1\,mA}}$$

Now,

$I_{DSS} = 1\,mA$, $I_{D_2} = ?$ $V_T = 1$ $V_{GS} = 3$

$$I_{D_2} = 1\times10^{-3}\left(1-\frac{3}{1}\right)^2 = \underline{\underline{4\,mA}}$$

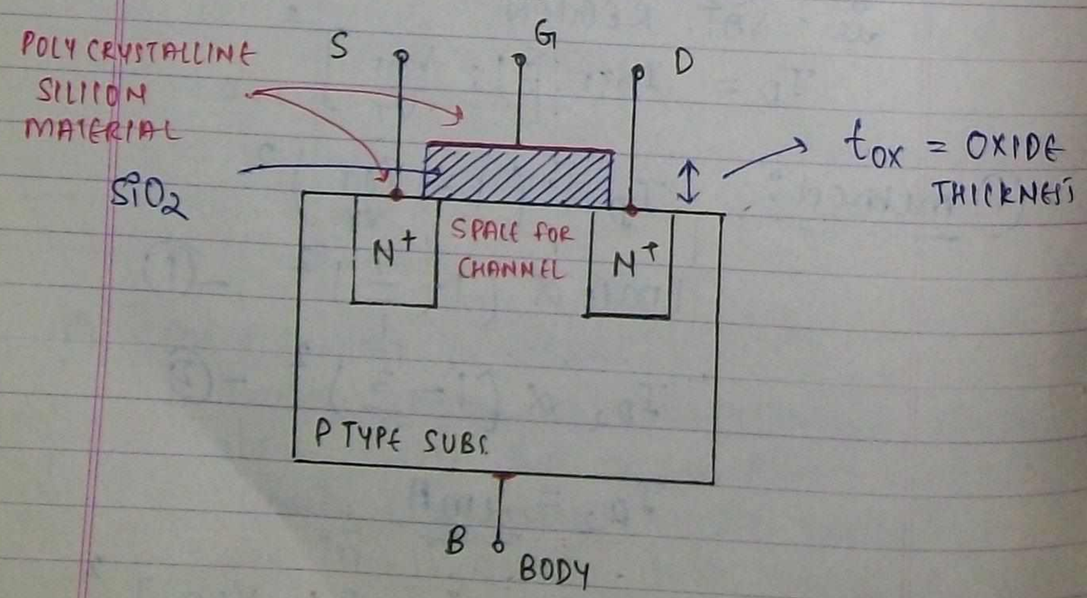
$I_D > I_{DSS}$ (enhancement mode)

③ <u>method</u> : In saturation region. (for E MOSFET ONLY)

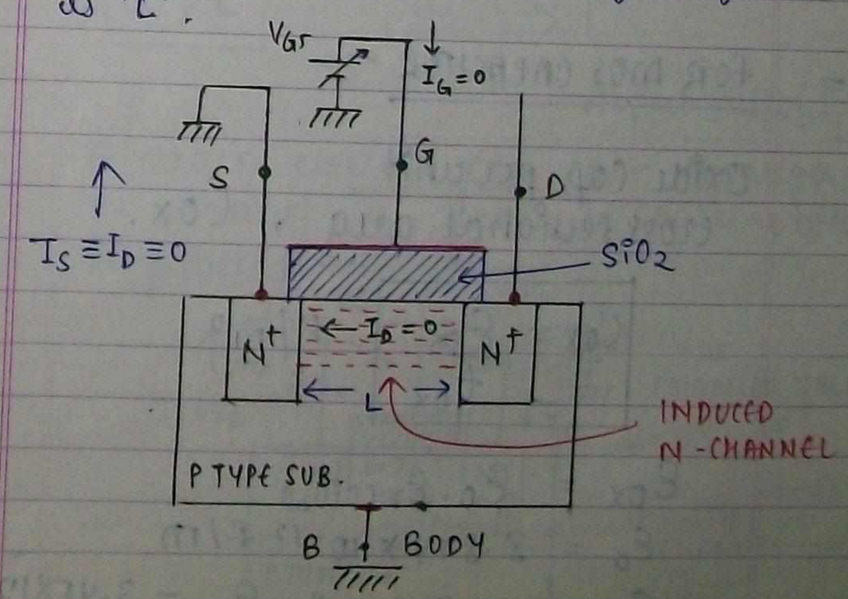
$$I_D = K\left[V_{GS} - V_T\right]^2$$

$$\frac{1\,mA}{I_{D_2}} = \frac{(2-1)^2}{(3-1)^2} \Rightarrow I_{D_2} = \underline{\underline{4\,mA}}$$

⇒ N-CHANNEL ENHANCEMENT MOSFET (E ONLY MOSFET) –



- E only MOSFET is a modern MOSFET
- In E-MOSFET there is no pre existing channel.
- In E-MOSFET Aluminimum plate or metallic plate are elliminated and in place of it polycrystalline Si material is provided.
- In modern MOSFET the material used for the gate is polycrystalline silicon.
- In E-MOSFET the channel can be created by applying proper gate to source voltage.
- When proper V_{GS} is applied at flat channel is induced in between the two N^+ regions and the length of channel is 'L'.



- when V_{GT} is applied this voltage is also appearing between gate and body of the mosfet and due to the electric field intensity ($\mathcal{E}$) the channel is induced in between the source and drain.

- The channel is a flat channel.

- In E only mosfet channel is induced channel.

- A parallel plate capacitance is created at the gate region with polycrystalline silicon gate and induced channel ~~as~~ as the two plates of capacitor & SiO_2 as the dielectric. The gate region is now working as a MOS capacitor.

- FOR MOS CAPACITOR –

Oxide Cap. per unit cross sectional area, C_{ox}.

$$C_{ox} = \frac{\mathcal{E}_{ox}}{t_{ox}} \quad f/m^2$$

$$\mathcal{E}_{ox} = \mathcal{E}_0 \cdot \mathcal{E}_{r(SiO_2)}$$

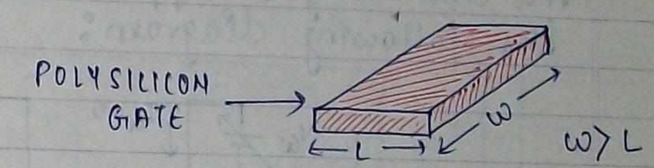
$$\mathcal{E}_0 = 8.854 \times 10^{-12} \ f/m$$

$$\mathcal{E}_{r(SiO_2)} = 3.9 \quad \therefore \mathcal{E}_{ox} = 3.45 \times 10^{-11} \ f/m$$

$$C_{ox} = \frac{3.45 \times 10^{-11}}{t_{ox}} \quad f/m^2$$

- GATE CAPACITANCE –

$$C_{GATE} = C_{ox} \cdot W \cdot L \quad f$$



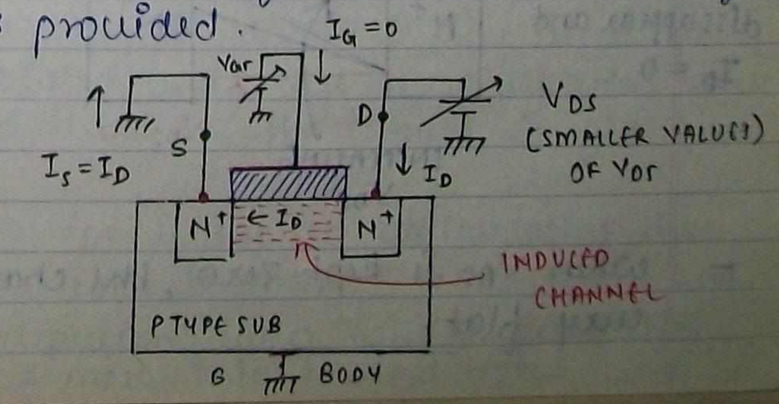
- L is the length of the channel and it is also equal to the length of the polycrystalline silicon gate.

- W = width of the polycrystalline Si gate

- $\boxed{W > L}$ $\quad \left(\frac{W}{L}\right) > 1$

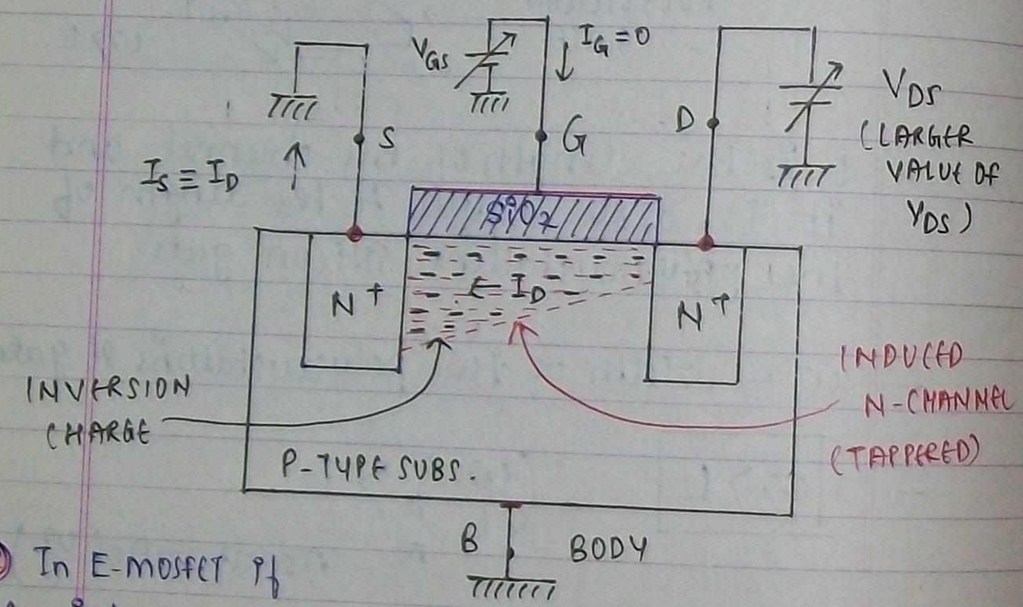
Aspect ratio $\left(\frac{W}{L}\right)$

- A drain current can pass through the channel if drain to source voltage is provided.

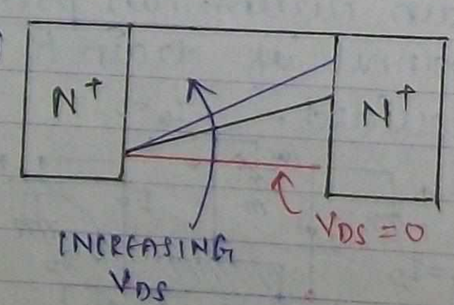


- when smaller values of V_{DS} is applied the drain current is very small and also the channel will remain almost flat as indicated in above diagram.

- when larger values of V_{DS} is applied, the channel gets tappered as given in the following diagram:

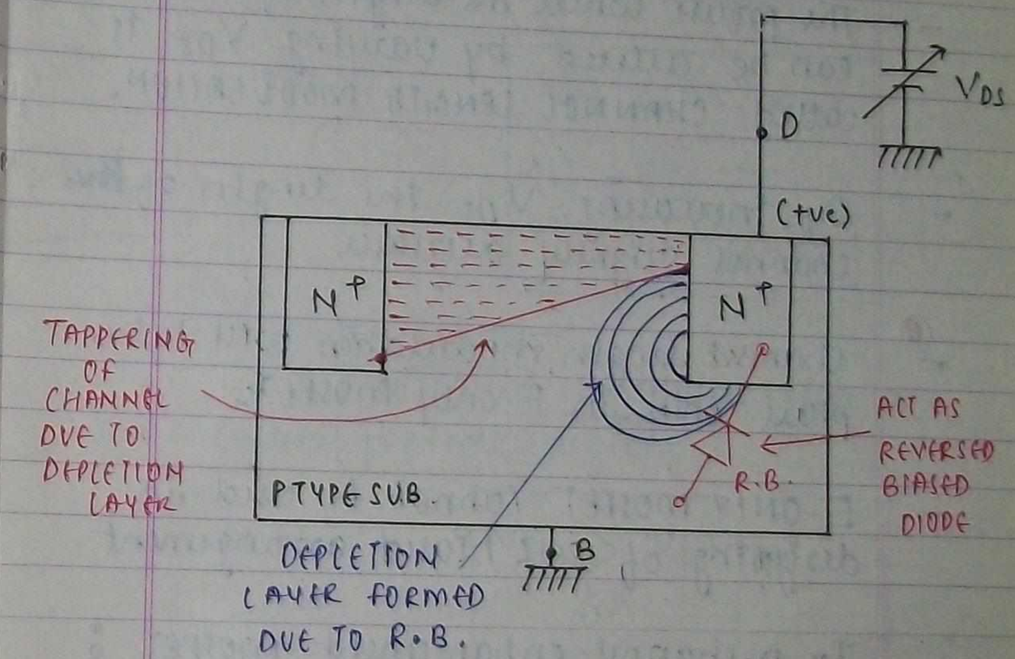


* In E-MOSFET if V_{GS} is kept zero then channel will disappear and $I_D = 0$



- when V_{DS} is kept zero, the channel is very flat.

- when V_{DS} is applied and increasing the channel gets tappered as given in fig.



- when V_{DS} is applied this voltage is also appearing between the drain and body of the MOSFET and this will be working as a reversed biased diode.

- when V_{DS} is kept zero, the diode is unbiased and there is no depletion layers and therefore the channel is flat.

- when V_{DS} is applied and increasing the diode will be more & more R.B. and the depletion layer will be penetrating more & more into the substrate and

Therefore the channel gets tapped as shown in above diagram.

- The process where the length of the channel can be altered by varying V_{DS} is called CHANNEL LENGTH MODULATION.

- By increasing V_{DS} the length of the channel slightly decreases.

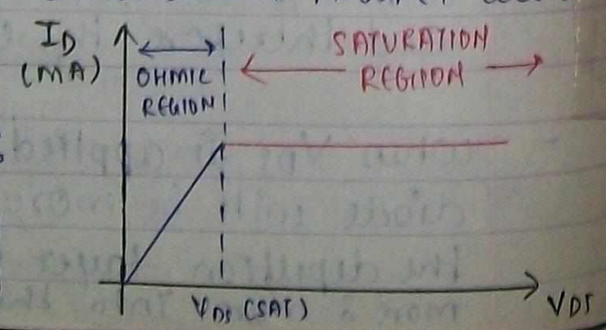
- (A) Channel length modulation will take place only in E only MOSFET.

- E-ONLY MOSFET cannot be used in designing of self biased arrangement.

- In n-channel enhancement MOSFET :
  1. Channel potential increases from source to drain.
  2. Inversion charge decreases from source to drain.

- The drain characteristic & transfer characteristic for n-channel enhancement MOSFET are :

(1) DRAIN CHARACTERISTICS :



where,
$V_{DS(SAT)} = [V_{GS} - V_T]$

OHMIC REGION –

- Also called linear region (or) Non saturation region. (or) triode region

- (A) Conditions :

$$V_{DS} < V_{DS(SAT)}$$
(or)
$$V_{DS} < [V_{GS} - V_T]$$

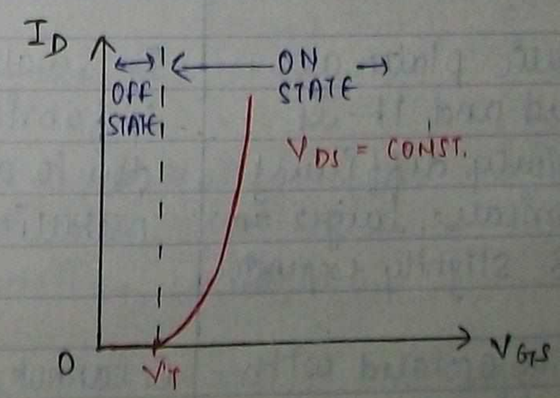
SATURATION REGION –

Also called Pinchoff region or called pentode region.

- (A) Condⁿ :

$$V_{DS} \geq V_{DS(SAT)}$$
(or)
$$V_{DS} \geq [V_{GS} - V_T]$$

(2) TRANSFER CHARACTERSTICS –



Now,

If, $\boxed{V_{GS} < V_T}$, MOSFET is OFF-STATE
ie O.C.

If, $\boxed{V_{GS} \geq V_T}$ MOSFET is ON STATE
ie S.C.

⇒ COMPARISON B/W DEPLETION MOSFET & E MOSFET.

DE-MOSFET	E MOSFET
1. There is pre existing channel.	1. ~~Pre~~ No Pre existing channel & the channel has to be created by apply proper V_{GS}.
2. Diffused channel	2. Induced channel.
3. Suitable to operated in depletion mode and enhancement mode.	3. Suitable only for enhancement mode.
4. No channel length modulation.	4. Channel length modn will exists.
5. metallic plate are provided and it is comparatively difficult to fabricate, larger in size & slightly expensive	5. Smaller in size, easy to fabricate & economical due to absence of the metallic plate.
6. Can be operated with self biased.	6. Cannot operated with self biased arrangement

⇒ THRESHOLD VOLTAGE OF THE MOSFET. – (V_T, V_t, V_{th})

– It is also called gate to source threshold voltage denoted by V_{GST}.

FIG: TRANSFER CHARACTERSTIC OF P-CHANNEL E MOSFET →

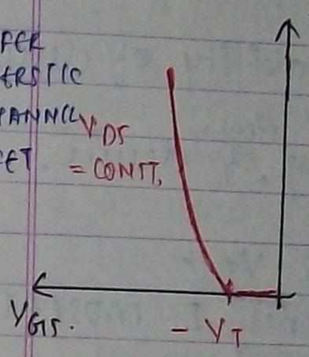
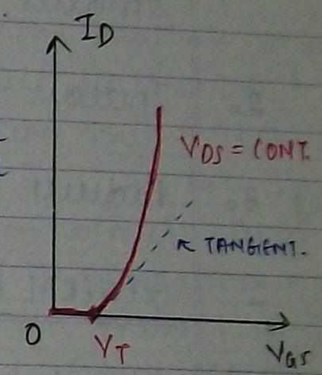


FIG: TRANSFER CHARACTERSTIC OF N CHANNEL E-MOSFET →



– for NMOS threshold voltage is positive & for PMOS threshold voltage is negative.

– Threshold voltage is defined as the min. gate to source voltage where the MOSFET enters into ON state.

– V_T is in the range of 0.5 V to 3 V.

– Typical value of V_T is 1 V.

– The threshold voltage of the MOSFET can be graphically obtained from transfer characteristic. (tangent).

– for better performance of the MOSFET the threshold voltage of the MOSFET must be as small as possible.

ADVANTAGES OF SMALLER V_T –

1. It enables the device to operate with smaller value of supply voltage.
2. Increase the compartability of device
3. Reduces the switching time of device.

GENERAL EQUATION FOR V_T –

for N-channel E-MOSFET the threshold voltage is –

$$V_T = V_{TO} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right]$$

where,

$$\gamma = \frac{\sqrt{2qN_A\varepsilon}}{C_{ox}} = \frac{t_{ox}\sqrt{2qN_A\varepsilon}}{3.45\times10^{-11}}$$

γ = fabrication process parameter.

N_A = acceptor conc. & it is doping conc. of P type substrate.

V_{SB} = substrate voltage.

ϕ_f = a physical parameter is also called fermi voltage (typ value = 0.6 V)

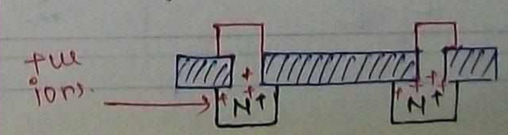
V_{TO} is the value of threshold voltage when substrate voltage is kept zero

- The threshold voltage of the MOSFET can be increased by increasing the substrate voltage.
- If a small variation in the substrate voltage V_{SB} will result a small variation in the threshold voltage and this will cause a small variation in I_D. ie the I_D is now controlled by substrate and therefore the substrate is now working as the second gate in the MOSFET and this mechanism is called BODY EFFECT of the MOSFET.

PROCEDURE TO REDUCE V_T –

- The threshold voltage of the MOSFET can be reduced by using any one of the following methods:

1. By using polycrystalline Si material replacing the aluminium plate so that work function of the material is reduced and also contact potential is reduced and this will reduce the threshold voltage.
2. By using ion implantation technique.



3. By reducing the doping conc. of the substrate material.

4. By increasing oxide capacitance (C_{ox}) per unit cross-sectional area.

5. By reducing oxide thickness (t_{ox}).

NOTE-

- Polycrystalline silicon is also called polysilicon.
- Silicon nitride can also be used in place of polysilicon crystalline silicon.

⇒ EQUATIONS FOR NMOS TRANSISTOR -

(1) OVER DRIVE VOLTAGE (V_{OV}) -

$$V_{OV} = V_{DS(SAT.)}$$

$$V_{OV} = [V_{GS} - V_T]$$

(2) OPERATION IN TRIODE REGION -

$V_{DS} < V_{DS(SAT)}$ or $V_{DS} < [V_{GS} - V_T]$

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

In the triode region drain ~~current~~ voltage (V_{DS}) is very small and therefore neglecting the higher terms,

$$I_D \simeq \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} \right]$$

let $\mu_n C_{ox} = k_n$ → Process transconductance Parameter (A/V^2)

$$I_D \simeq k_n \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} \right]$$

let $k_n \left(\frac{W}{L}\right) = k_n'$ → constant (A/V^2)

$$I_D = k_n' \left[(V_{GS} - V_T) V_{DS} \right]$$

- The above equation represent a first order equation and therefore in the triode Region I_D exhibits a linear relationship

- In the triode region drain to source resistance (r_{DS}) (or) channel resistance are given :

$$r_{DS} = \frac{V_{DS}}{I_D} \quad \Omega$$

$$\boxed{r_{ds} = \frac{1}{k_n'(V_{GS}-V_T)}} \ \Omega$$

$$\boxed{r_{ds} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)}} \ \Omega$$

- In the triode region r_{ds} can be altered by varying V_{GS}. and therefore the FET is now working as a voltage variable resistor.

- In the triode region FET can work as VVR (voltage variable resistor) by varying gate to source voltage.

- In the triode region, the transconductance g_m is:

$$\boxed{g_m = \frac{\partial I_D}{\partial V_{GS}}}$$

and $I_D = k_n'[V_{GS}-V_T]V_{DS}$

$$\frac{\partial I_D}{\partial V_{GS}} = k_n' \cdot V_{DS}$$

$$\boxed{g_m = k_n' V_{DS}} \quad \text{or} \quad \boxed{g_m = \mu_n C_{ox}\frac{W}{L} V_{DS}}$$

(Saturation region)

③ OPERATION IN PENTODE REGION -

$V_{DS} \geq V_{DS(SAT)}$. (or) $V_{DS} \geq [V_{GS}-V_T]$

$$\boxed{I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)[V_{GS}-V_T]^2}$$

$$\boxed{I_D = \frac{1}{2}k_n\left(\frac{W}{L}\right)[V_{GS}-V_T]^2}$$

let $\frac{1}{2}k_n\left(\frac{W}{L}\right) = k \rightarrow$ constant (A/V^2)

$$\boxed{I_D = k[V_{GS}-V_T]^2}$$

- In the saturation region I_D represent a second order eqn and this indicate I_D increases as a parabolic variation with V_{GS}.

- In the saturation region:

$$\boxed{g_m = \frac{\partial I_D}{\partial V_{GS}}}, \quad I_D = k[V_{GS}-V_T]^2$$

$$\frac{\partial I_D}{\partial V_{GS}} = 2k[V_{GS}-V_T]$$

$$\boxed{g_m = 2k\left[V_{GS} - V_T\right]} \quad \mho$$

$$g_m = 2 \times \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \left[V_{GS} - V_T\right]$$

$$\boxed{g_m = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[V_{GS} - V_T\right]} \quad \mho$$

⇒ EQUATION OF PMOS TRANSISTOR –

(1) OVERDRIVE VOLTAGE (V_{OV}) –

$$V_{OV} = V_{DS(SAT)}$$

$$V_{OV} = \left[V_{GS} - V_T\right]$$

(2) OPERATION IN TRIODE REGION –

$V_{DS} \ngtr V_{DS(SAT)}$ (or) $V_{DS} > \left[V_{GS} - V_T\right]$

$$\boxed{I_D = \mu_p C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}\right]}$$

$$\boxed{I_D \simeq \mu_p C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS}\right]}$$

let $\mu_p C_{ox} = k_p$ → process transcond^n parameter (A/V^2)

$$\boxed{I_D \simeq k_p \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS}\right]}$$

let $k_p \left(\frac{W}{L}\right) = k_p'$ → constant (A/V^2)

$$\boxed{I_D \simeq k_p' \left[(V_{GS} - V_T) V_{DS}\right]}$$

– DRAIN TO SOURCE resistance

$$r_{ds} = \frac{V_{DS}}{I_D}$$

$$\boxed{r_{ds} = \frac{1}{k_p' (V_{GS} - V_T)}} \quad \Omega$$

$$\boxed{r_{ds} = \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)}} \quad \Omega$$

– Transconductance

$$\boxed{g_m = \frac{\partial I_D}{\partial V_{GS}}} \quad \& \quad I_D = k_p' \left[V_{GS} - V_T\right] V_{DS}$$

$$g_m = k_p' V_{DS}$$

(or) $$\boxed{g_m = \mu_p C_{ox} \left(\frac{W}{L}\right) V_{DS}}$$

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(3) OPERATION IN SATURATION REGION -

$V_{DS} \leq V_{DS(SAT)}$ (OR) $V_{DS} \leq [V_{GS} - V_T]$

$$I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right) [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} k_p \left(\frac{W}{L}\right) [V_{GS} - V_T]^2$$

let $\frac{1}{2} k_p \left(\frac{W}{L}\right) \rightarrow k \rightarrow$ constant (A/V^2)

$$I_D = k [V_{GS} - V_T]^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad \& \quad I_D = k [V_{GS} - V_T]^2$$

$$\frac{\partial I_D}{\partial V_{GS}} = 2k [V_{GS} - V_T]$$

$$g_m = 2k [V_{GS} - V_T]$$

$$g_m = \mu_p C_{ox} \left(\frac{W}{L}\right) [V_{GS} - V_T]$$

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Pending :

(1) Hall voltage derivation

(2) Derivation for $W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) V_0}$

(3) Brief introductor to IC fabrication.

(4) prob. solving E MOSFET